

Compal Confidential

GOG10

DIS M/B Schematic Document

Intel Tiger Lake- H35 Processor with DDR4 SoDIMM + GN20-P0/P1

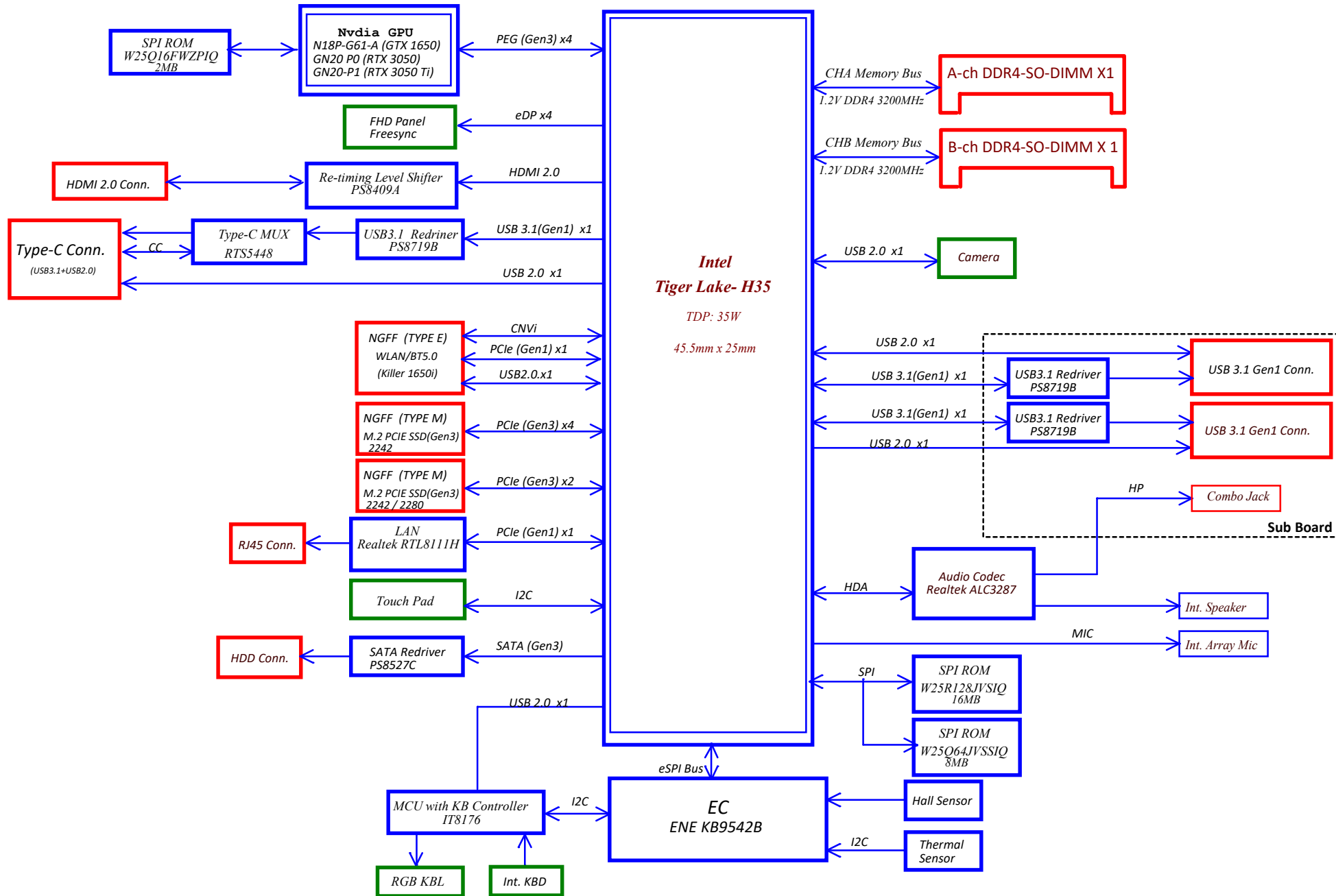
2020-09-15

LA-L161P

REV : 0.1

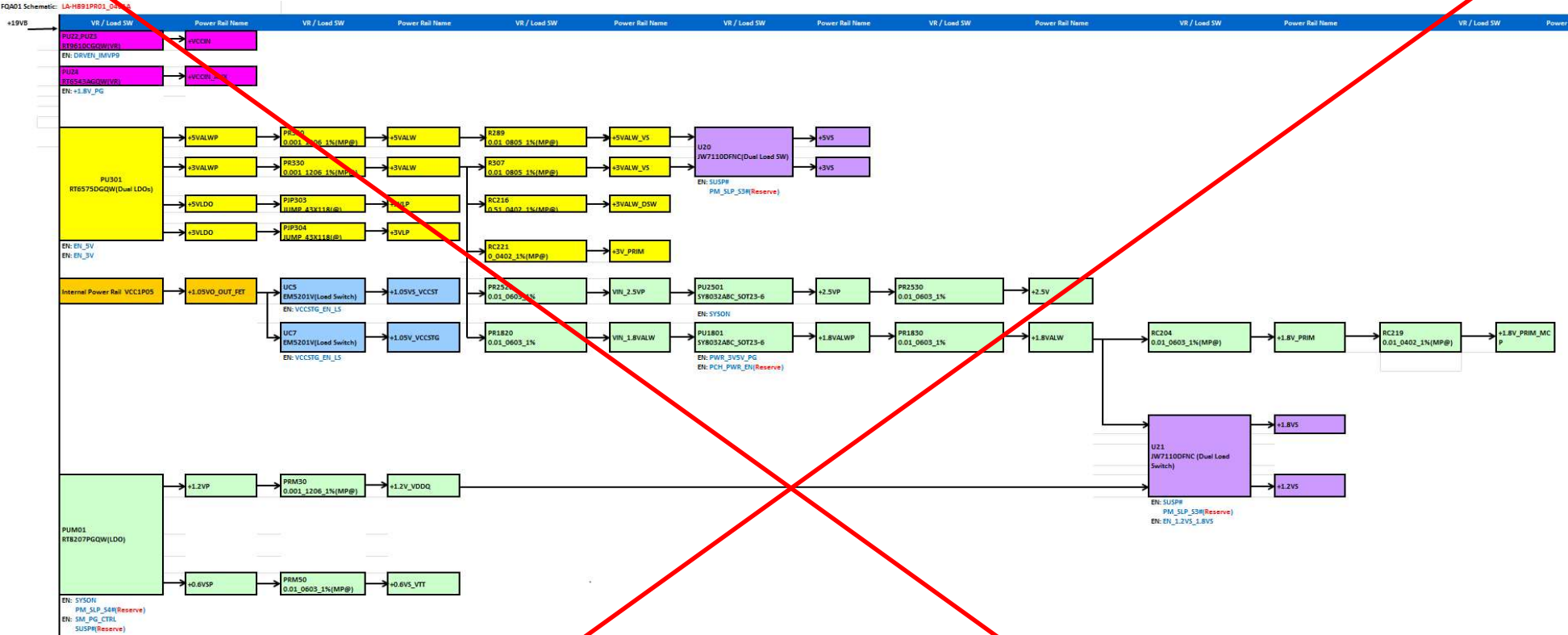
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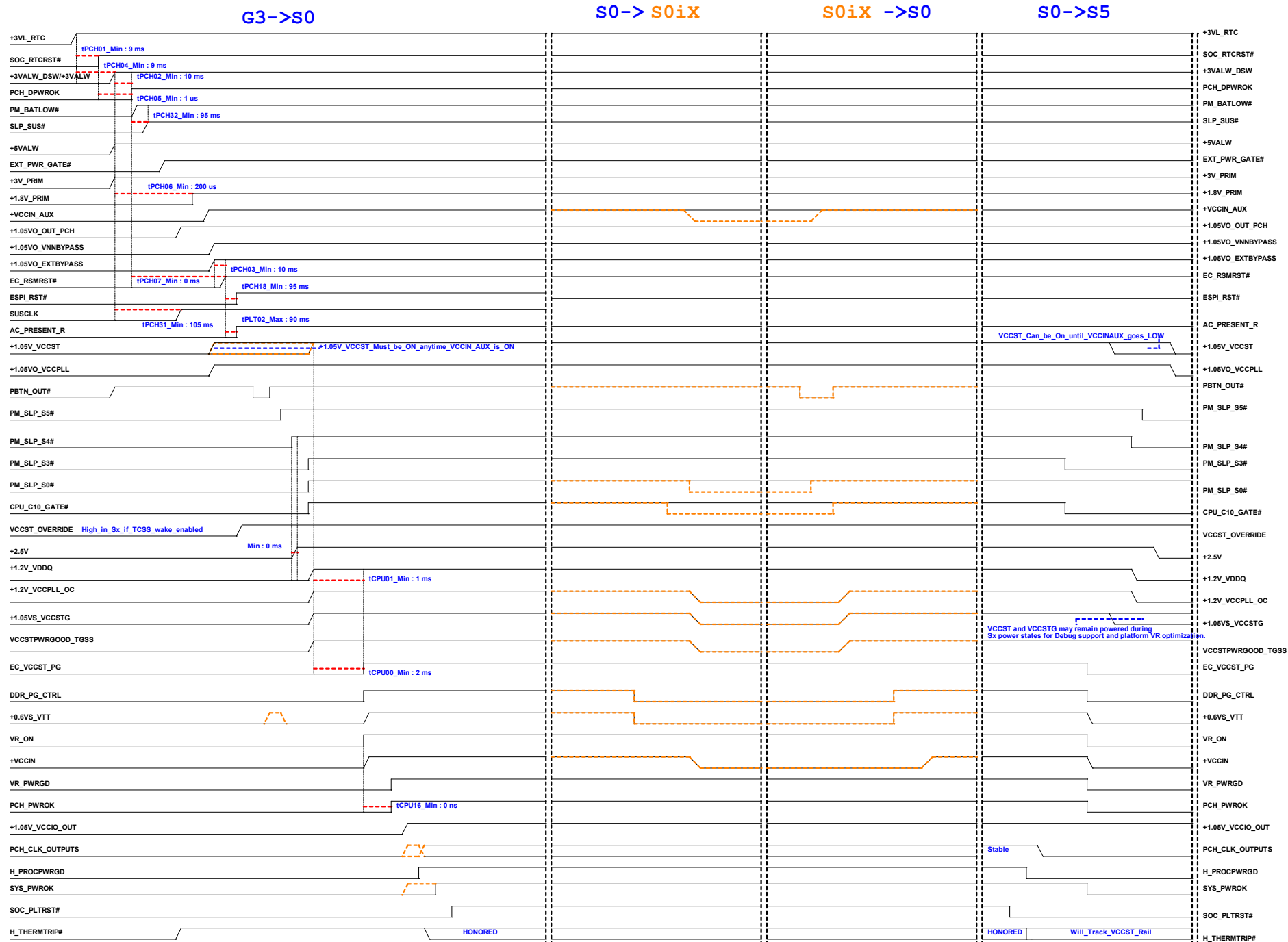
TGL-H35 Block Diagram



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[FQA01-Power Map_TGL-UP3_DDR4_Volume_S0ix]





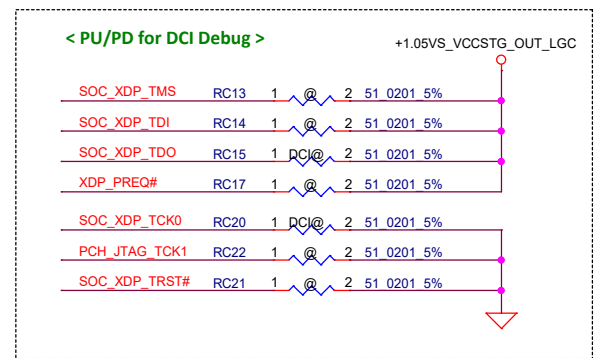
CPU



Table 32. USB3/USB2 Port Pairing for USB-C* Connectors

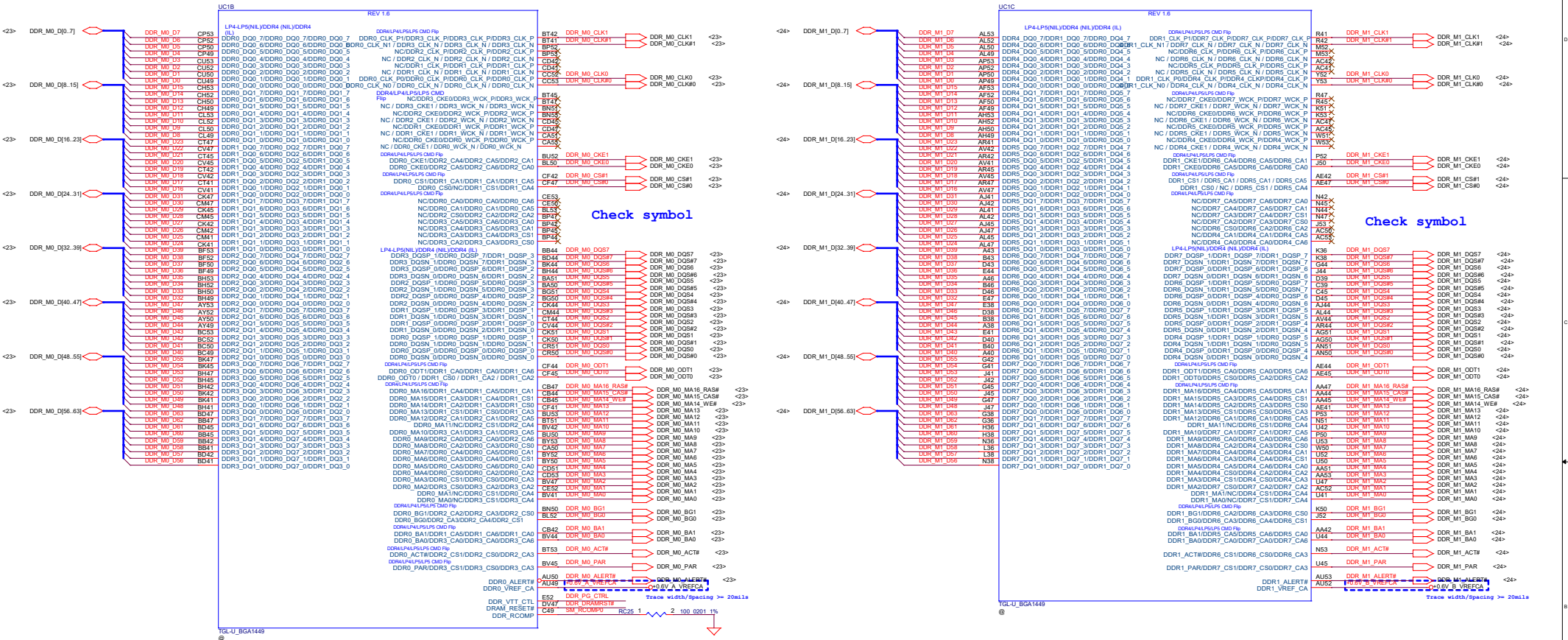
	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

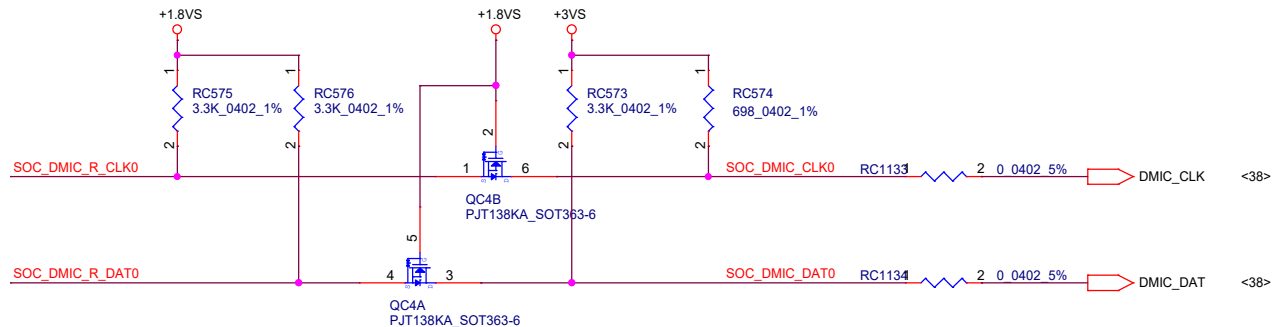
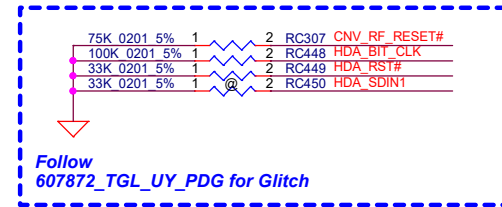
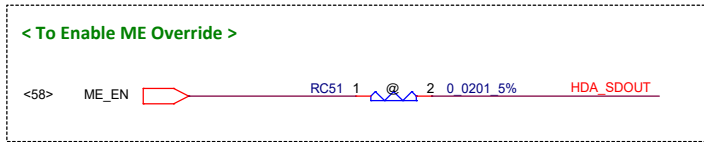
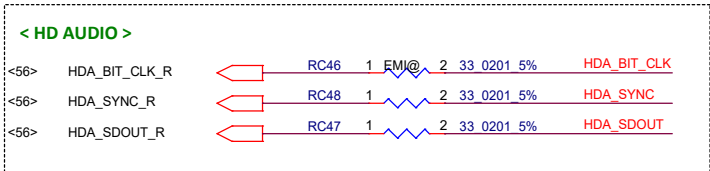
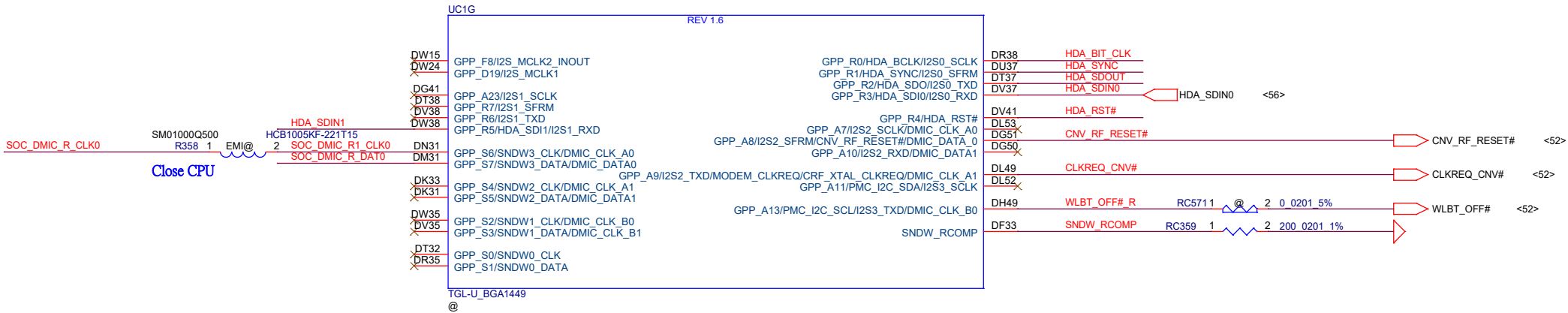
To make split xDCI controller working functionally for different USB-C* connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C* connectors, but it is not strictly required.



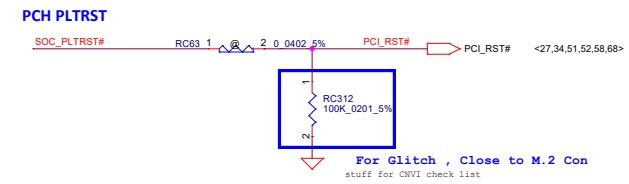
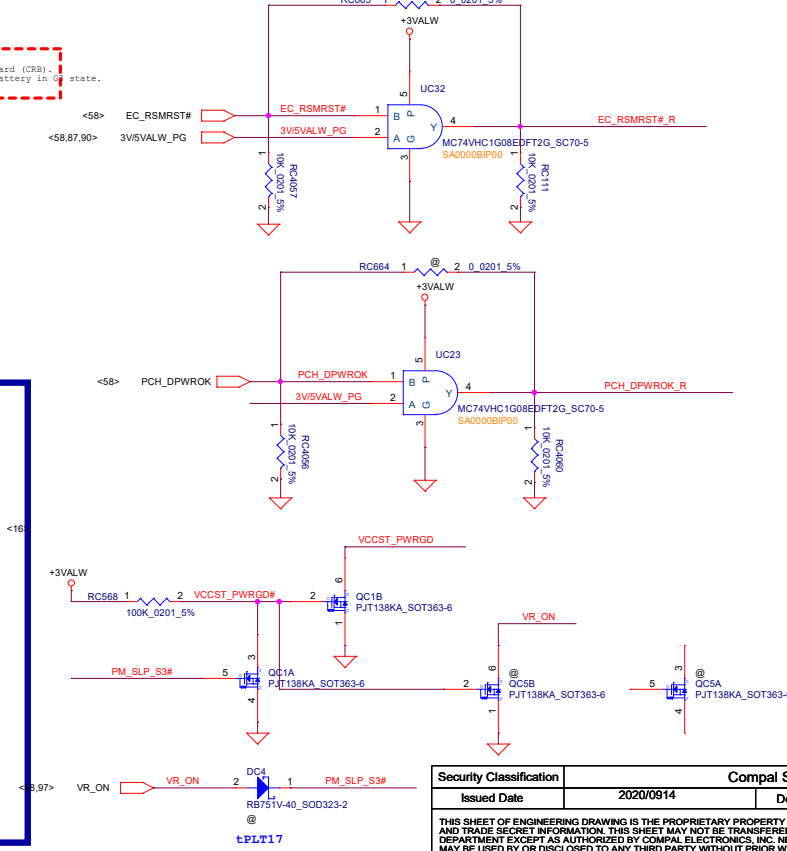
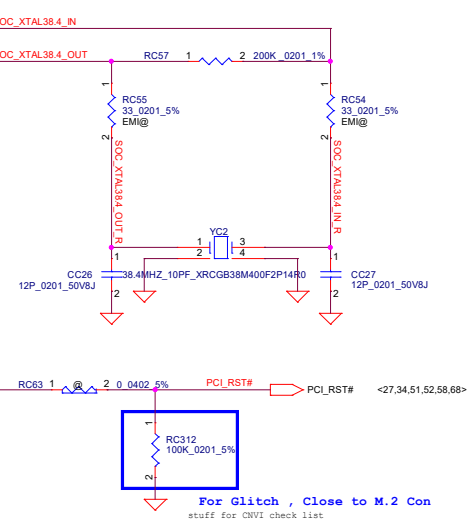
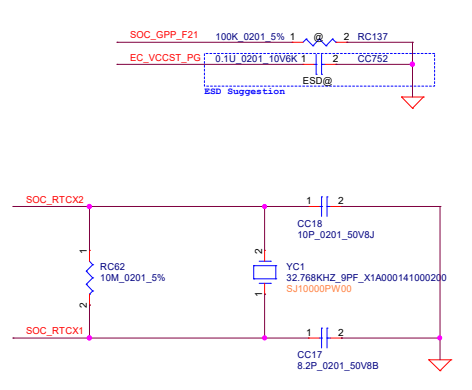
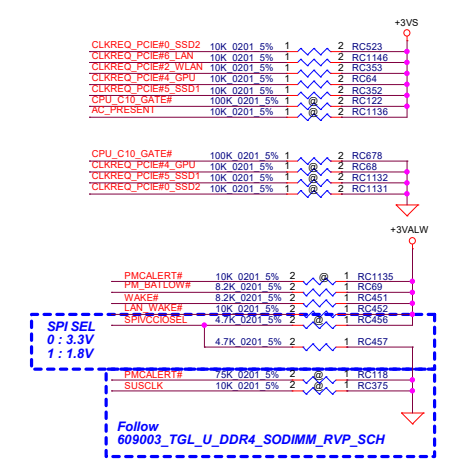
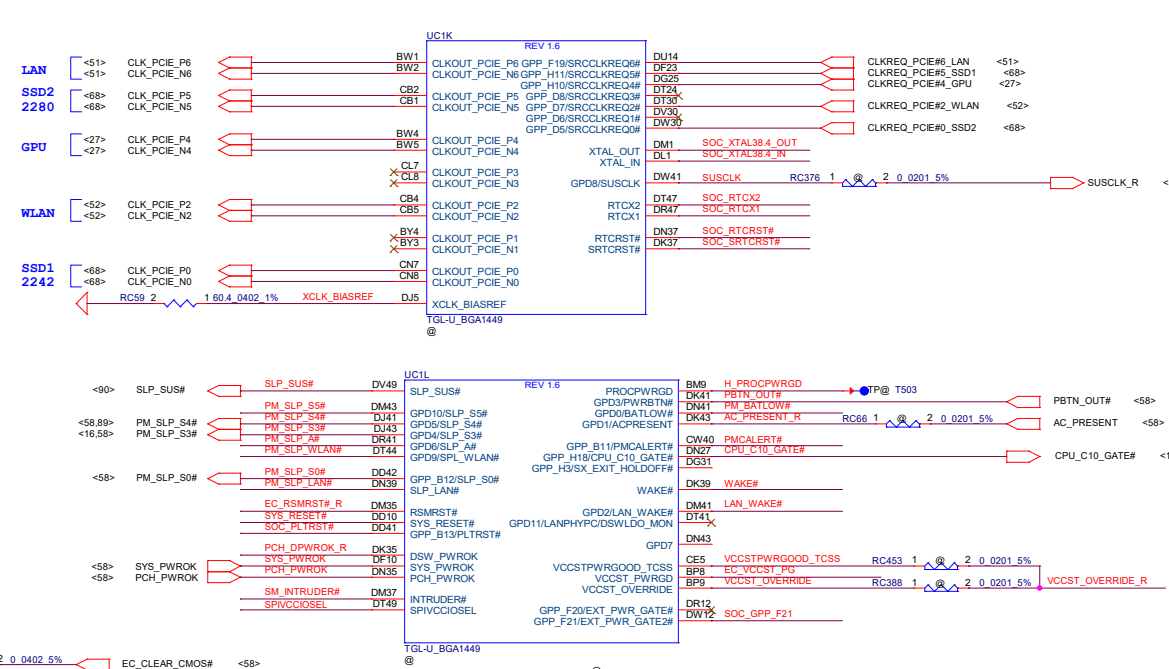
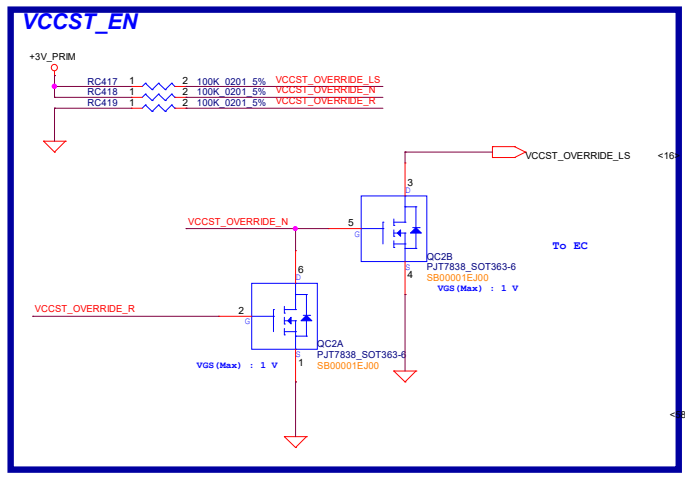
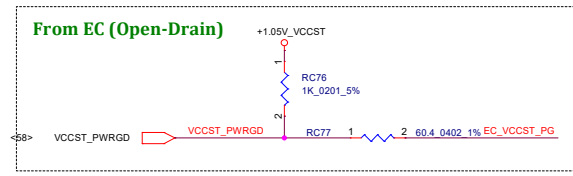
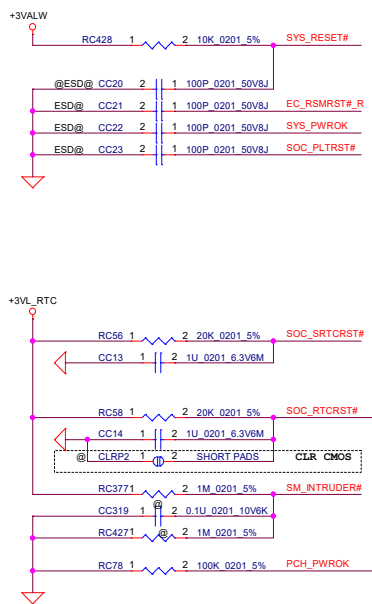
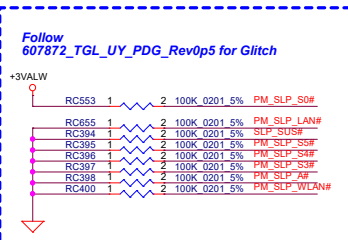
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Follow Intel DDR4 NIL

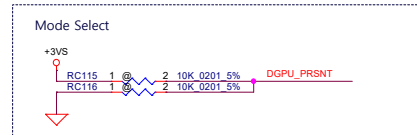
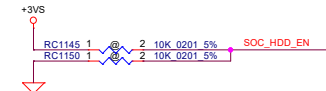
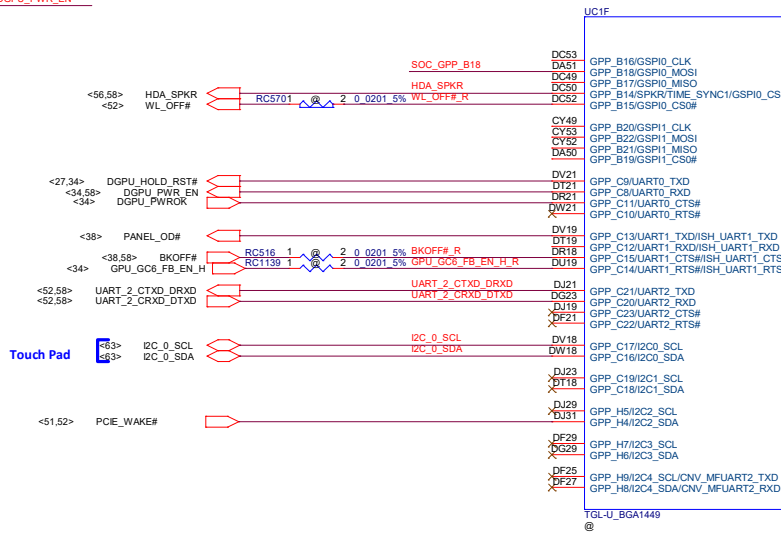
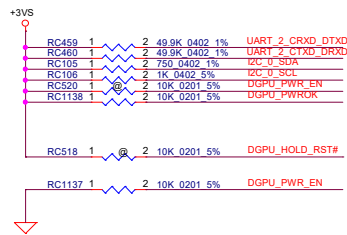




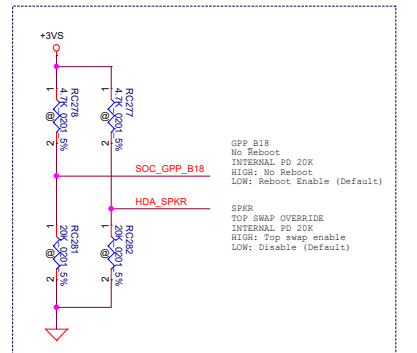
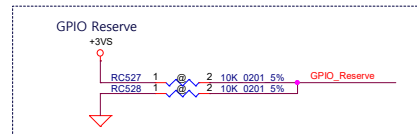
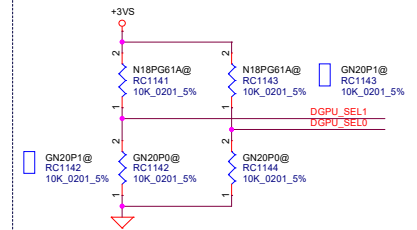
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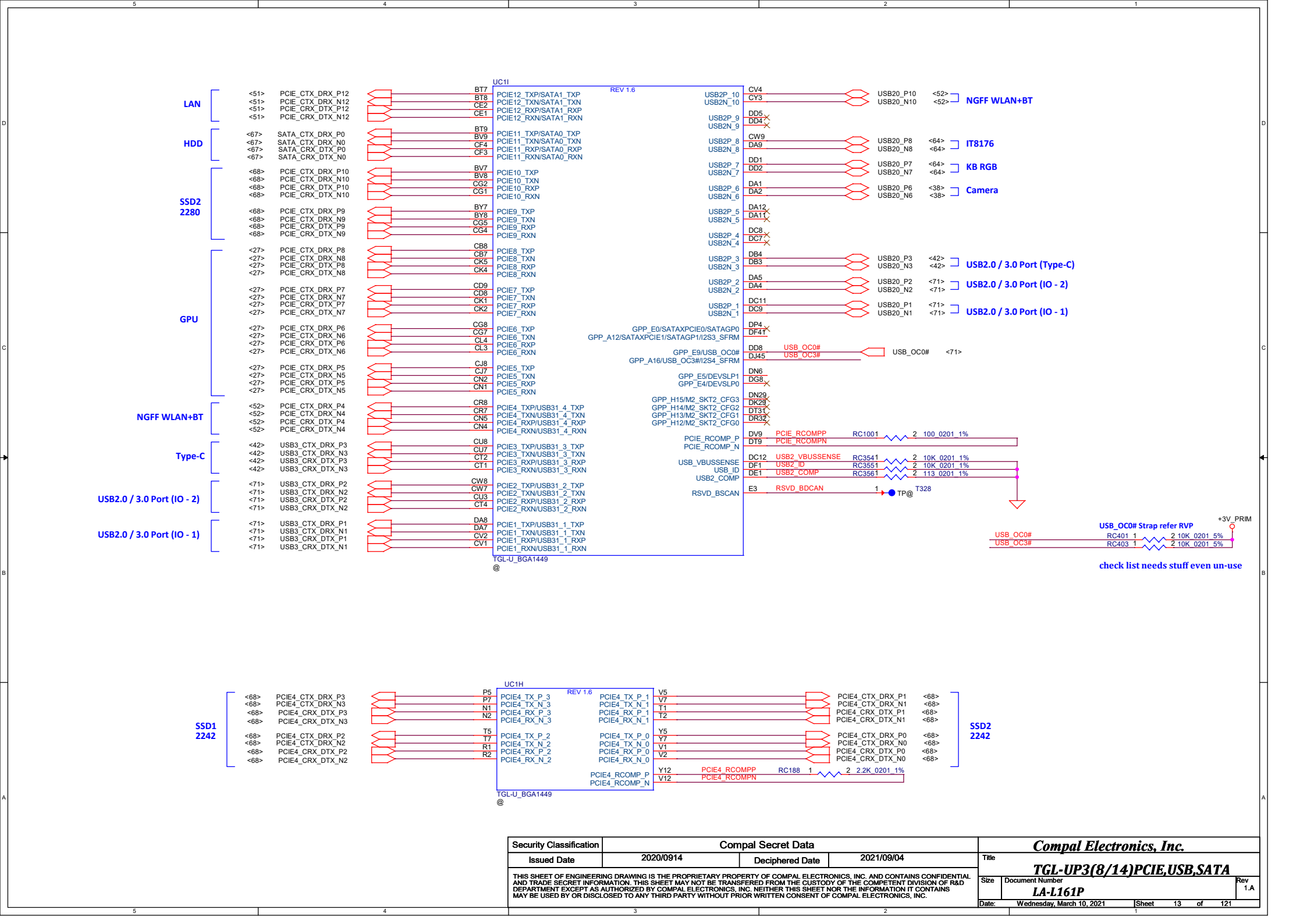


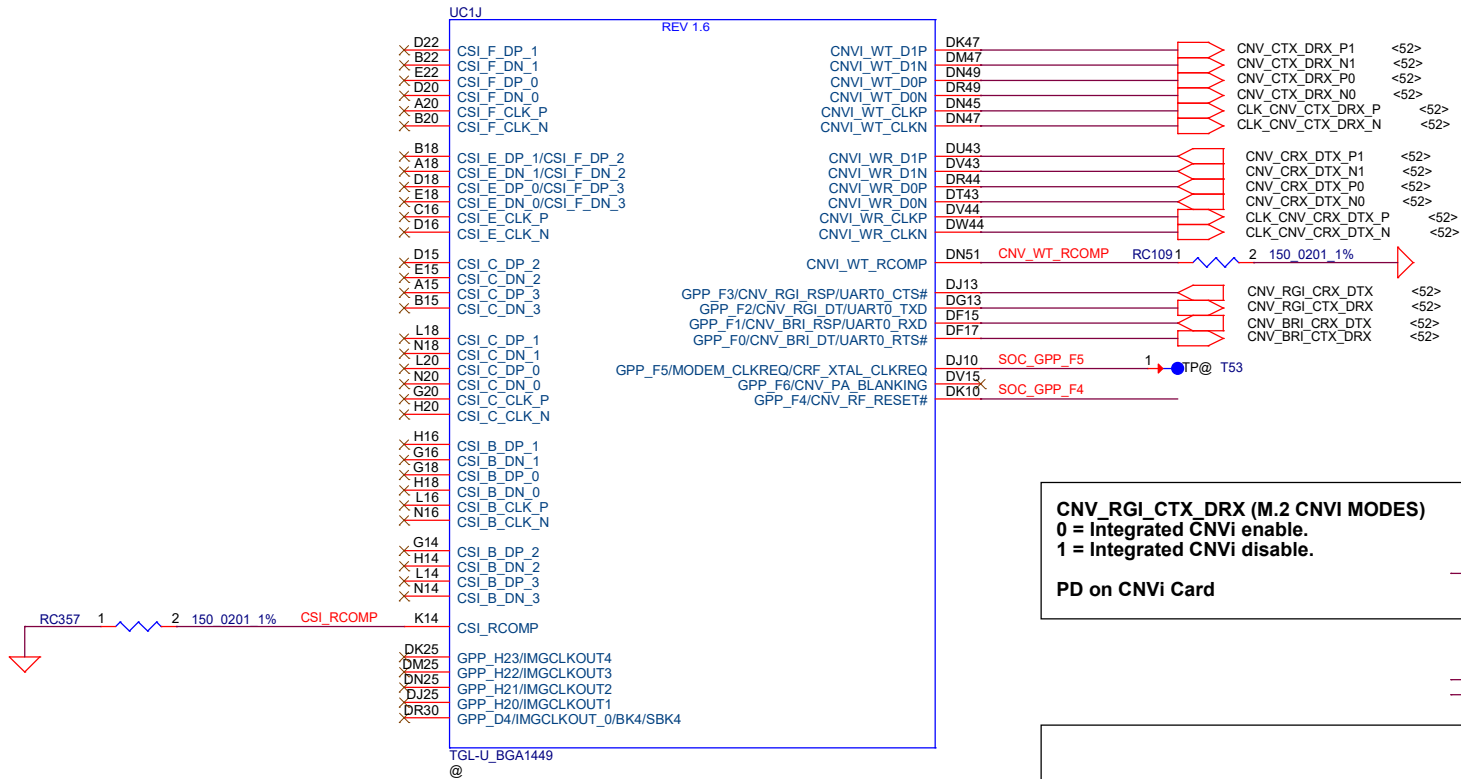
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GPU	DGPU_SEL1 (GPP_D1)	DGPU_SEL0 (GPP_D0)
GN20-P0	0	0
GN20-P1	0	1
N18P-G61-A	1	1







CNV_RGI_CTX_DRX (M.2 CNVi MODES)
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

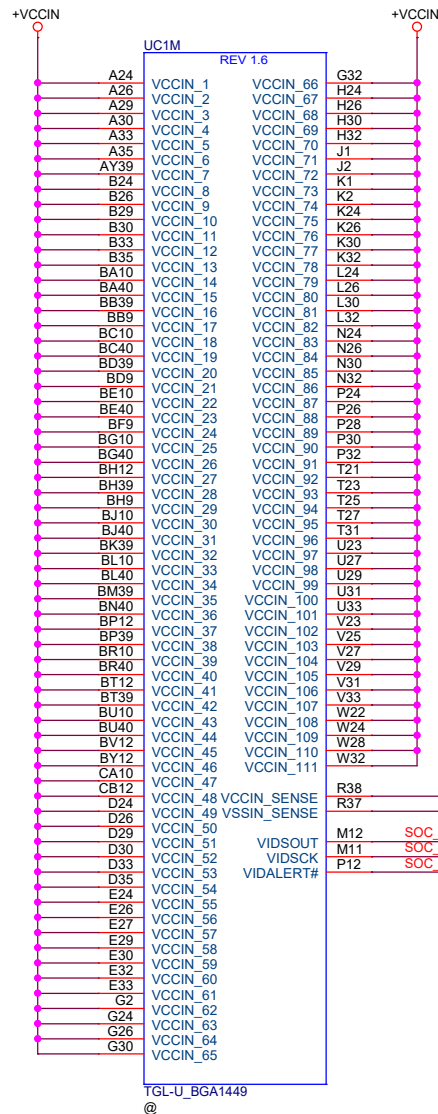
PD on CNVi Card

CNV_BRI_CTX_DRX (XTAL SEL)

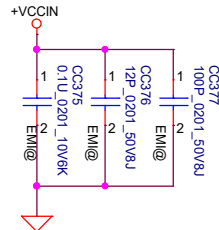
0 = 38.4/19.2MHZ (DEFAULT)
1 = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

WEAK INTERNAL PD 20K

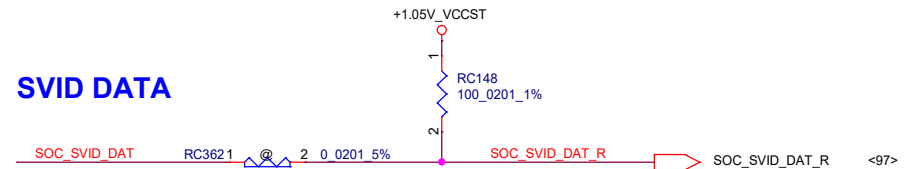
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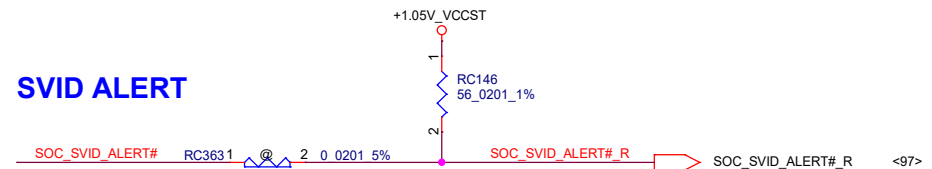
EMI CAPS-PLACE < 5mm from SOC VCCIN



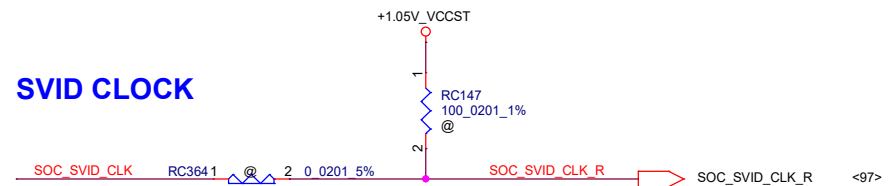
SVID DATA



SVID ALERT

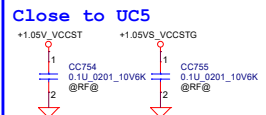
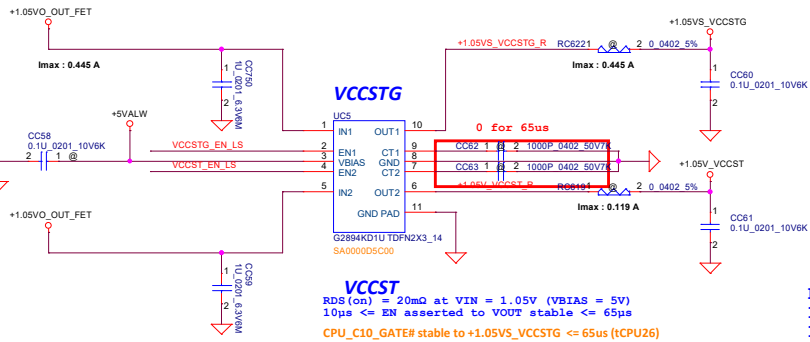
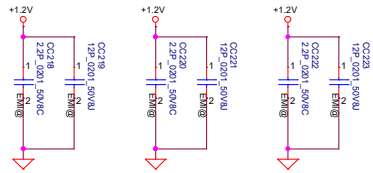


SVID CLOCK

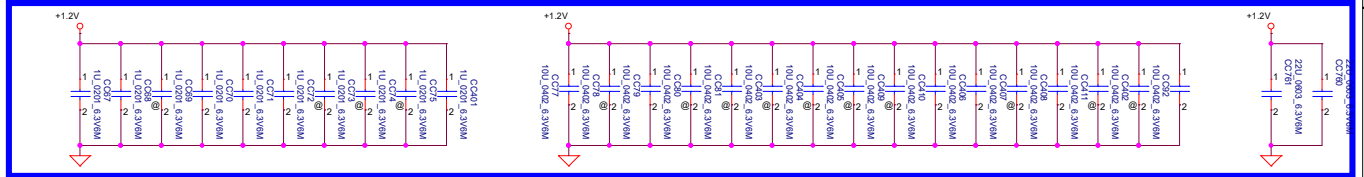


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EMI CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMI@)
2.2pF* 3 (EMI@)



Place on CPU Side
1uF* 10
10uF* 16
47uF * 2



VCCST/VCCSTG Enable

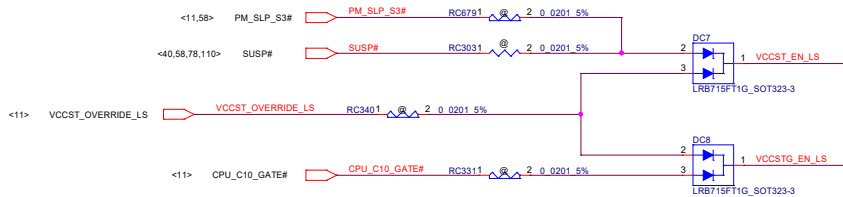


Figure 228. VCCST Enable Logic

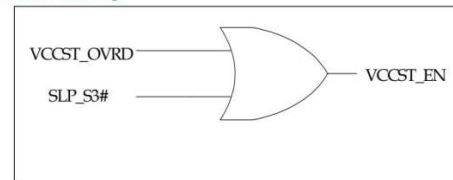
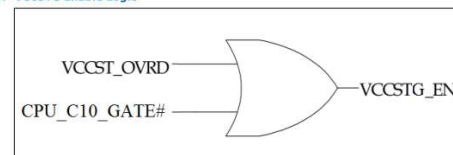
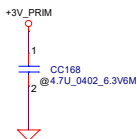
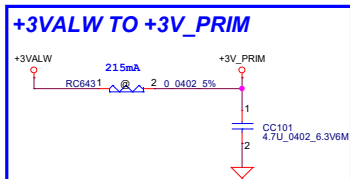
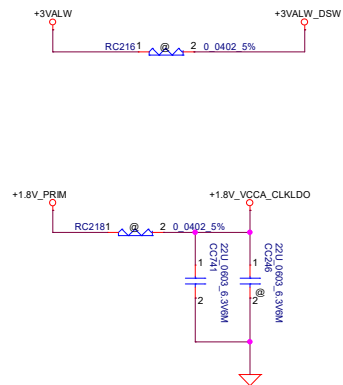


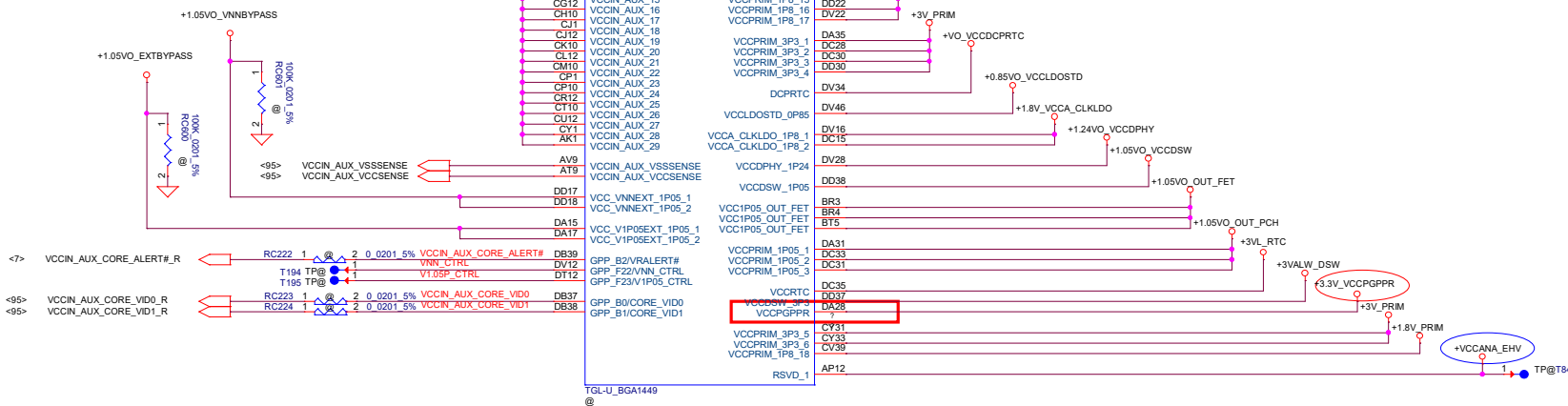
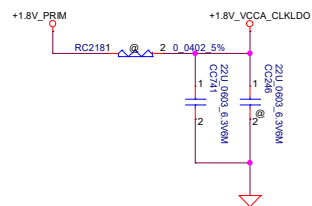
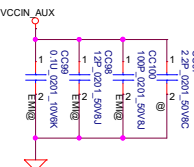
Figure 229. VCCSTG Enable Logic



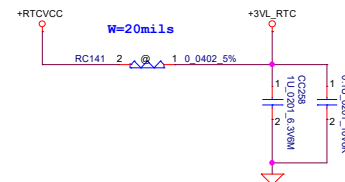
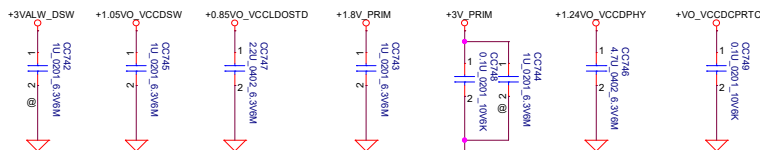


Package size

EMI CAPS-IN-PLACE
< 5mm from SOC VCCIN_AUX



NOTE:
576591-tgl-pch-lp-eds-vol1of2-rev0p5
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO.
607872_TGL_UY_PDG_Rev0p5
When configured as 3.3V or 1.8V, VCCPGPPR can be merged directly with
either VCCPRIM_1P8 or VCCPRIM_3P3 depending on their operating voltage.



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RC233 1 2 1K 0201 5% CFG4

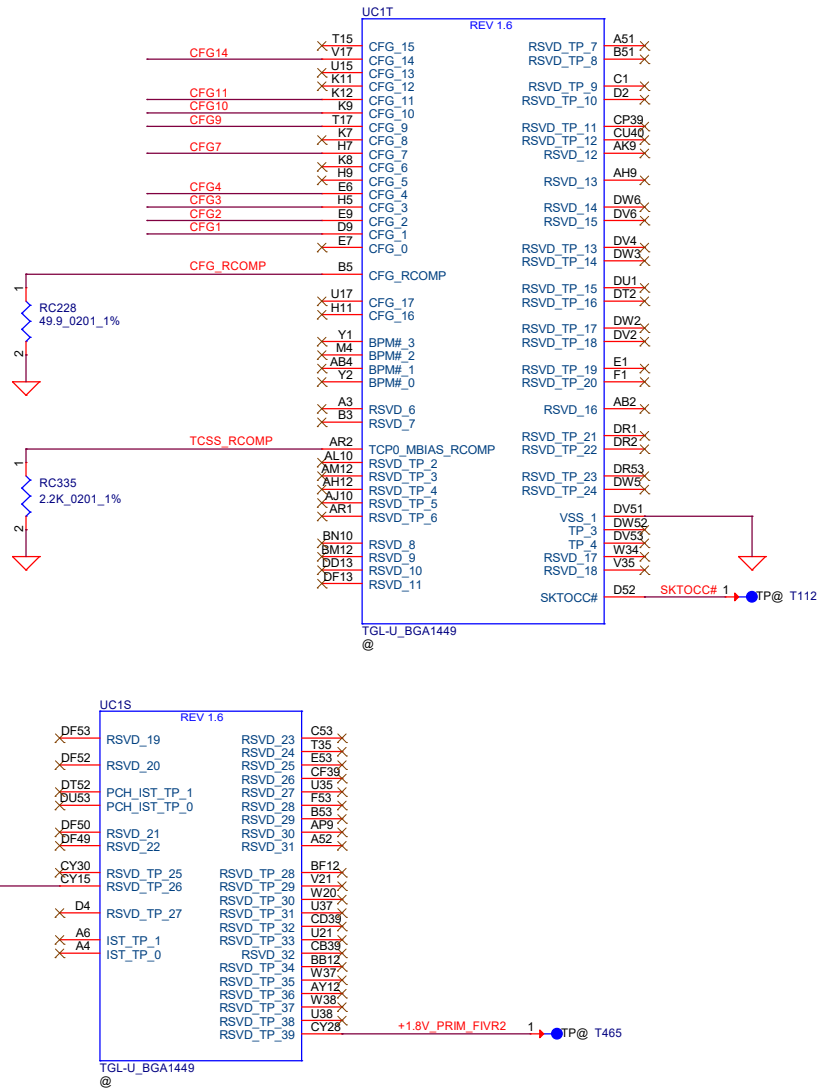
CFG4
Display port presence strap
LOW : Enable
An external display port device is connected to
the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port

+1.05V_VCCIO_OUT

RC250 1 2 1K 0201 5% CFG1
RC251 1 2 1K 0201 5% CFG2
RC252 1 2 1K 0201 5% CFG3
RC259 1 2 10K 0201 5% CFG7
RC262 1 2 1K 0201 5% CFG9
RC264 1 2 1K 0201 5% CFG10
RC266 1 2 1K 0201 5% CFG11
RC271 1 2 10K 0201 5% CFG14

RC642 1 2 10K 0201 5% CFG7
RC647 1 2 10K 0201 5% CFG14

CFG Signals
(For Strap & XDP)



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5	4	3	2	1
D				D
C				C
B				B
A				A
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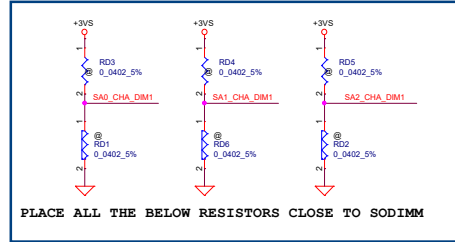
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D				D
C				C
B				B
A				A
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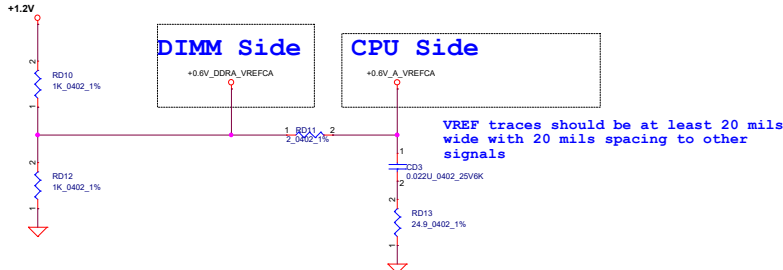
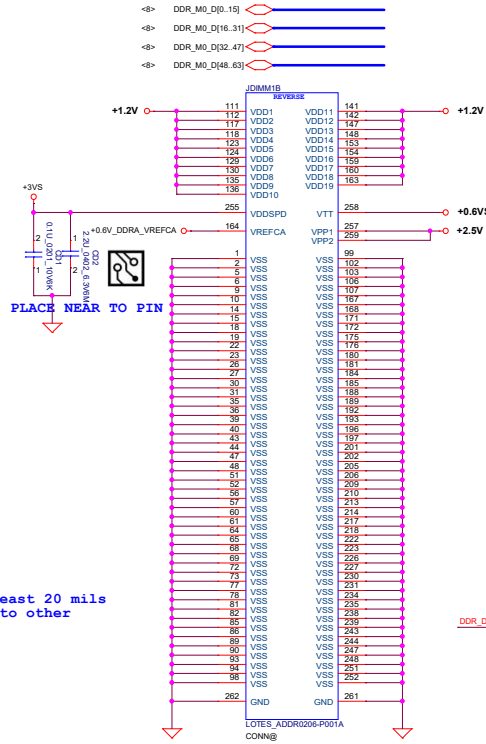
CHANNEL-M0

TOP: JDIMM1 CONN Non-ECC DIMM

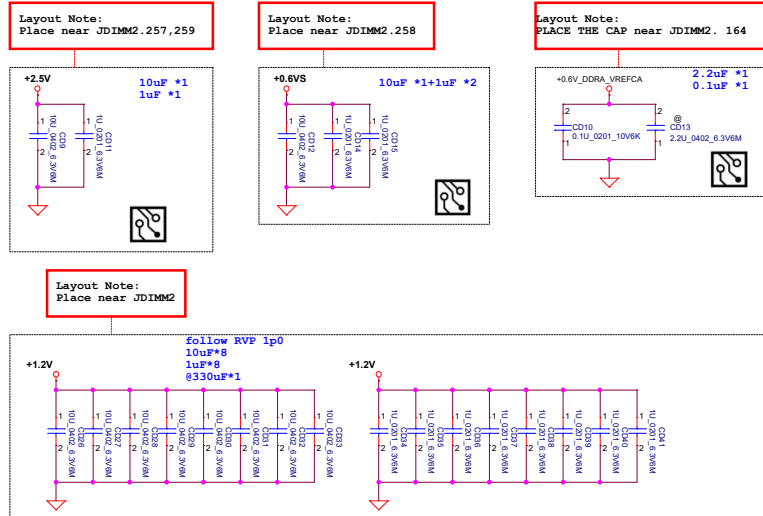


SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

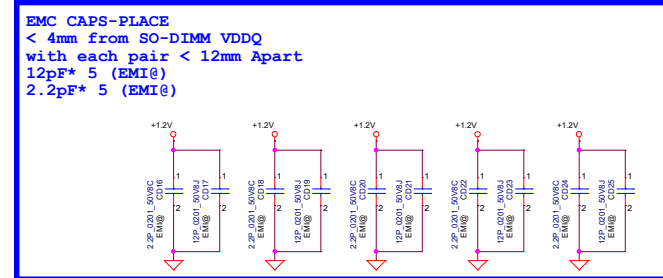
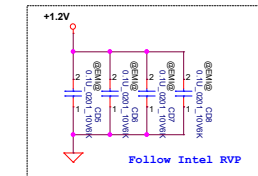
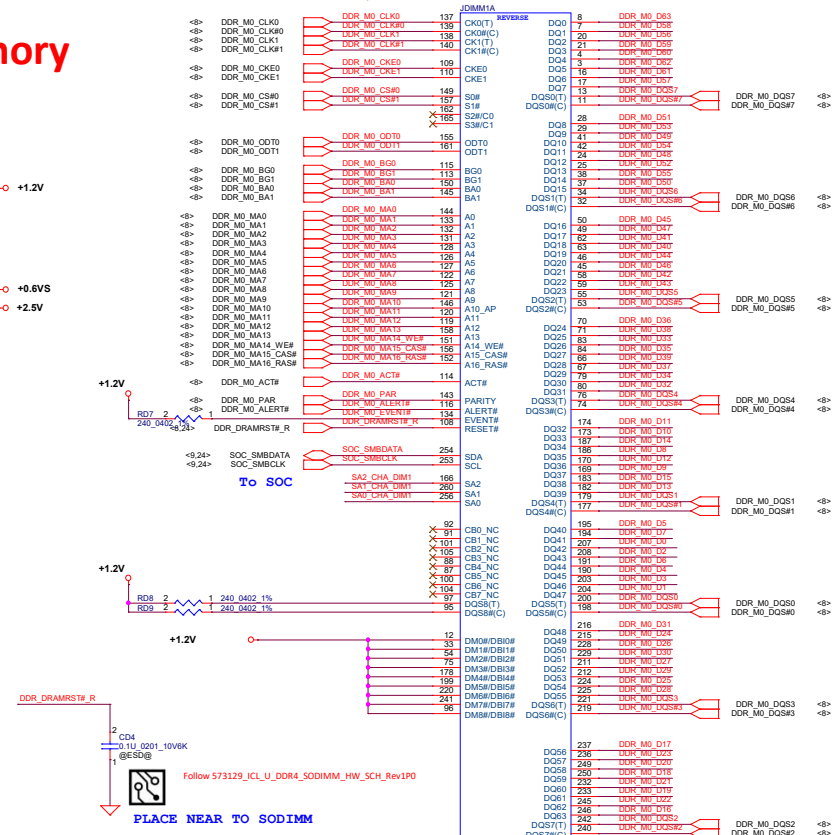
Non-Interleaved Memory



Decoupling Cap_Channel A

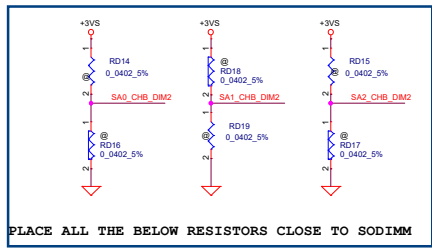


Reverse (4 mm), the same with Y750 DDR CONN

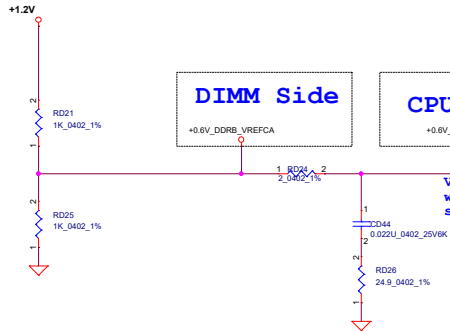


CHANNEL-M1

TOP: JDIMM2 CONN Non-ECC DIMM



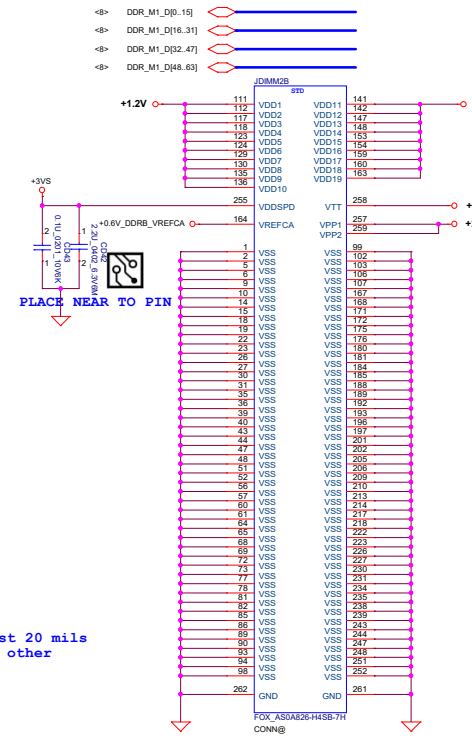
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S



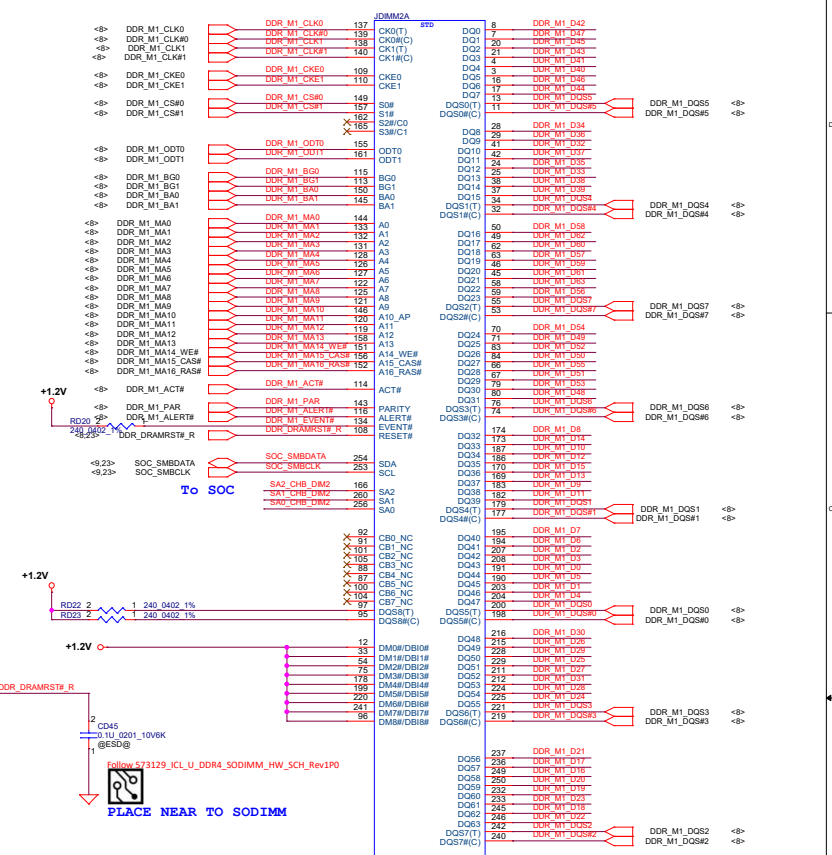
CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Non-Interleaved Memory

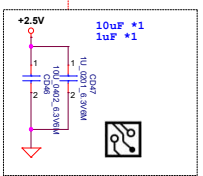


STD (4 mm), the same with Y750 DDR CONN

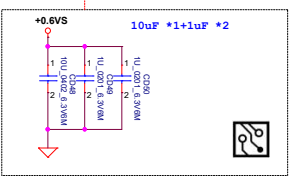


Decoupling Cap_Channel B

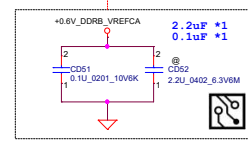
Layout Note:
Place near JDIMM1.257,259



Layout Note:
Place near JDIMM1.258



Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1

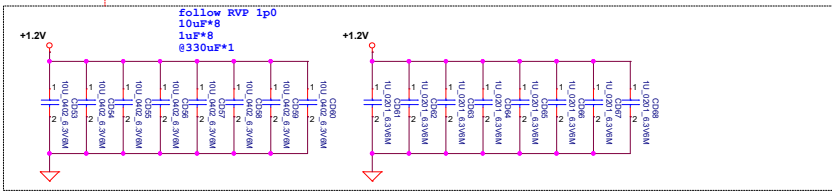


Table 50. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
DDR4 SODIMM 1DPC	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10 μ F (0603)
		Place on VTT plane close to DIMM	4x 1 μ F (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10 μ F (0603)
	VDDSPD	DIMM pin side, 1 per DIMM	2x 1 μ F (0402)

Note: 1. Total quantity is referring to 2 channels.

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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				Sheet	25 of 121
				Rev	1.A

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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				Rev	1.A

GC OFF 1.0 GPU Power ON/OFF

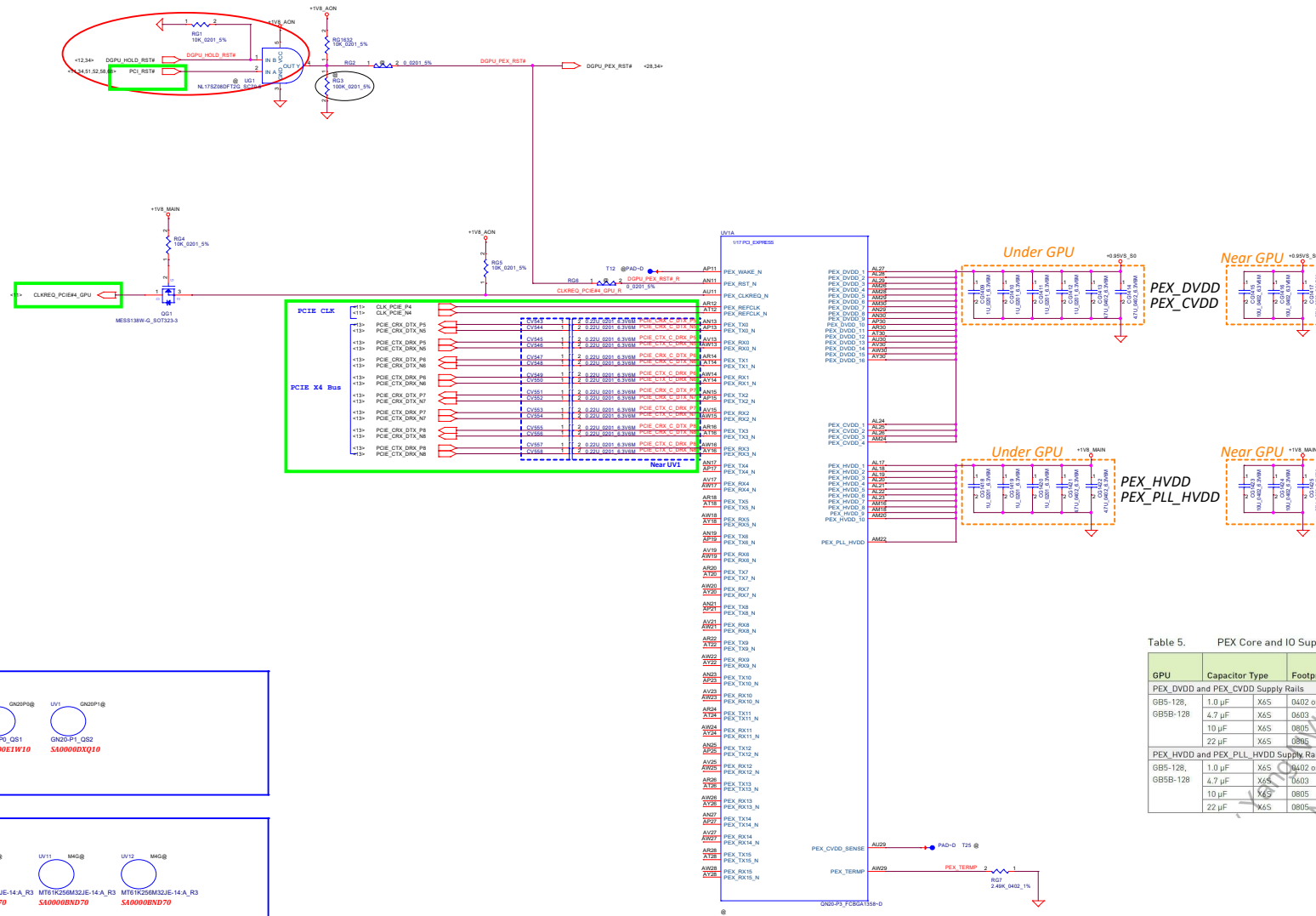
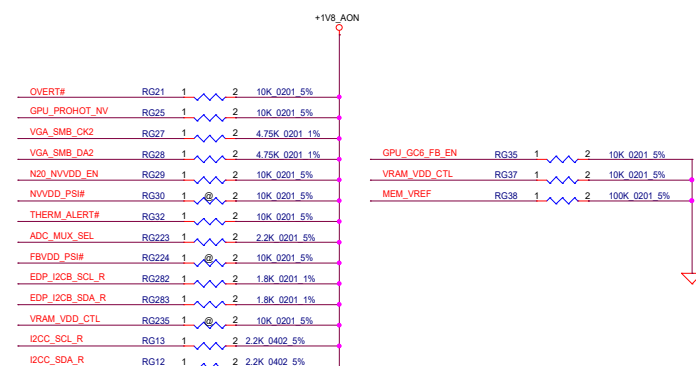
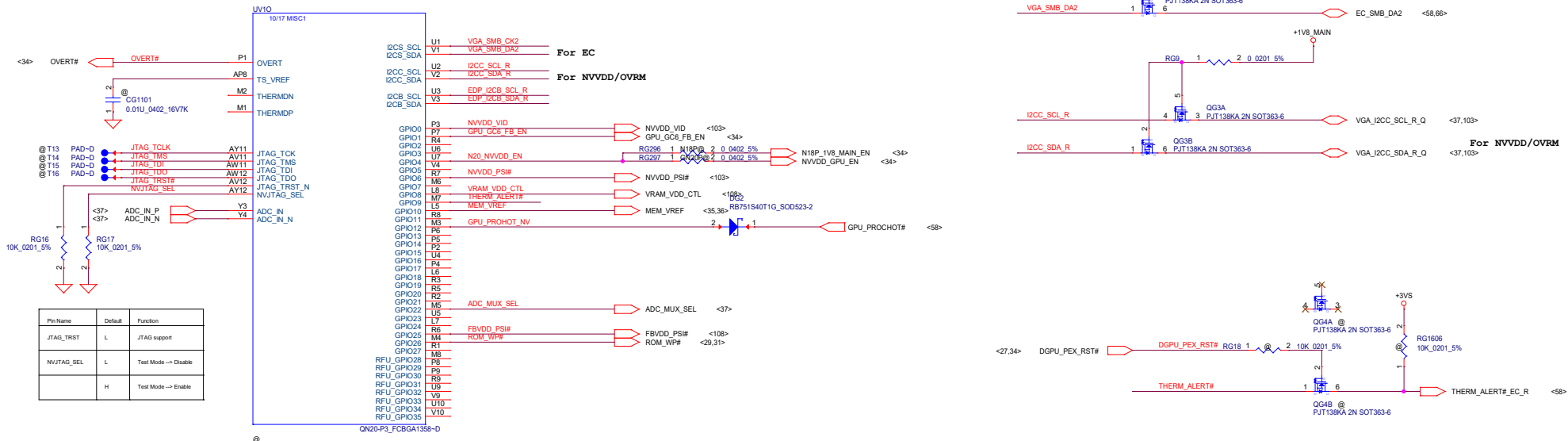
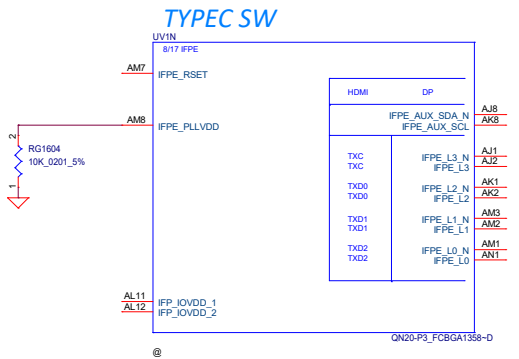
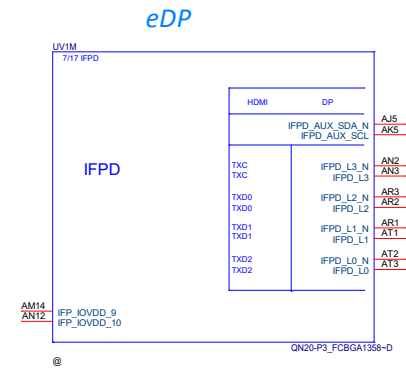
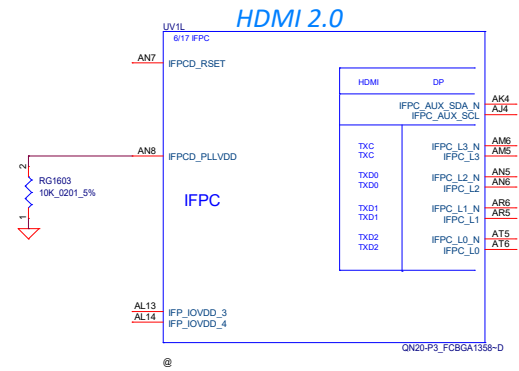
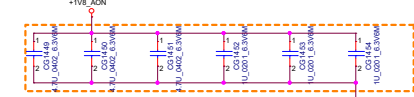
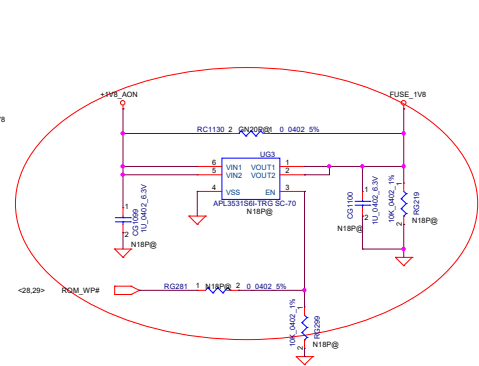
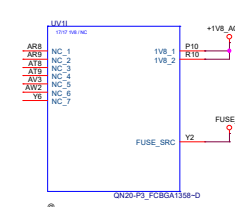
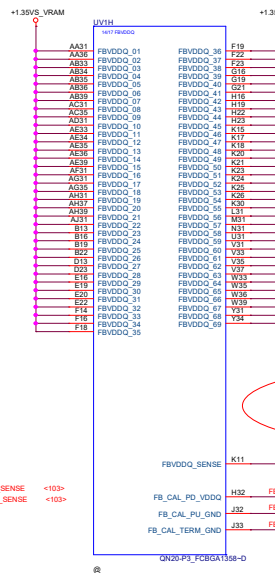
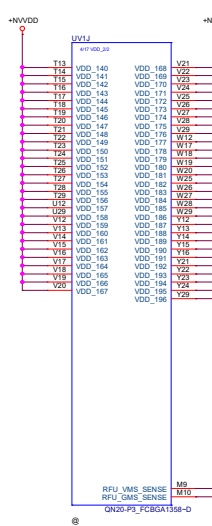
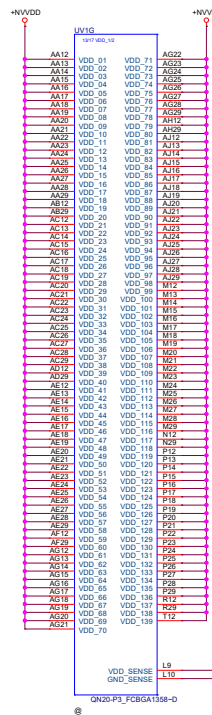
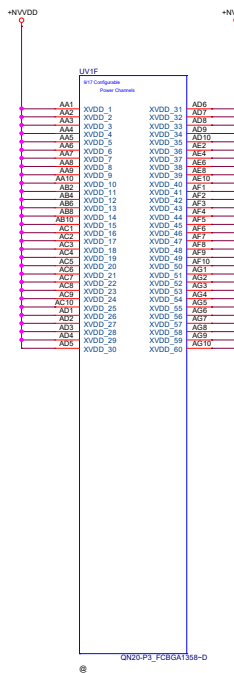


Table 5. PEX Core and IO Supply Decoupling and Filtering

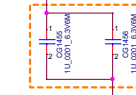
GPU	Capacitor Type	Footprint	Population		Location	
			GB5-128	GB5B-128		
PEX_DVDD and PEX_CVDD Supply Rails						
GB5-128, GB5B-128	1.0 μ F	X65	0402 or 0201W	4	2	Under GPU
	4.7 μ F	X65	0603	2	2	Under GPU
	10 μ F	X65	0805	2	2	Near GPU
	22 μ F	X65	0806	1	1	Near GPU
PEX_HVDD and PEX_PLL_HVDD Supply Rails						
GB5-128, GB5B-128	1.0 μ F	X65	0402 or 0201W	3	3	Under GPU
	4.7 μ F	X65	0603	2	2	Under GPU
	10 μ F	X65	0805	2	2	Near GPU
	22 μ F	X65	0805	1	1	Near GPU





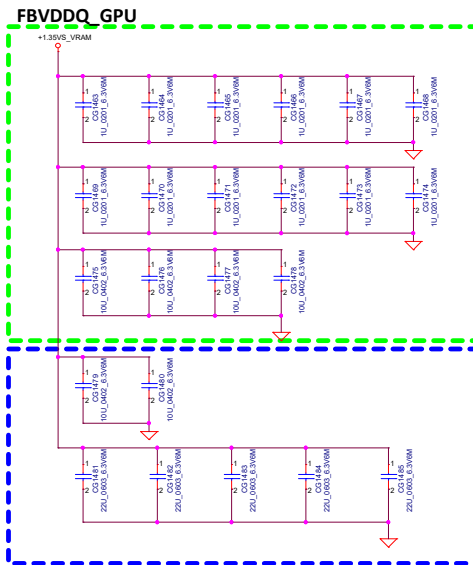


Near GPU



Under GPU

GPU Decoupling - NV Spec Recommendation



Place under GPU

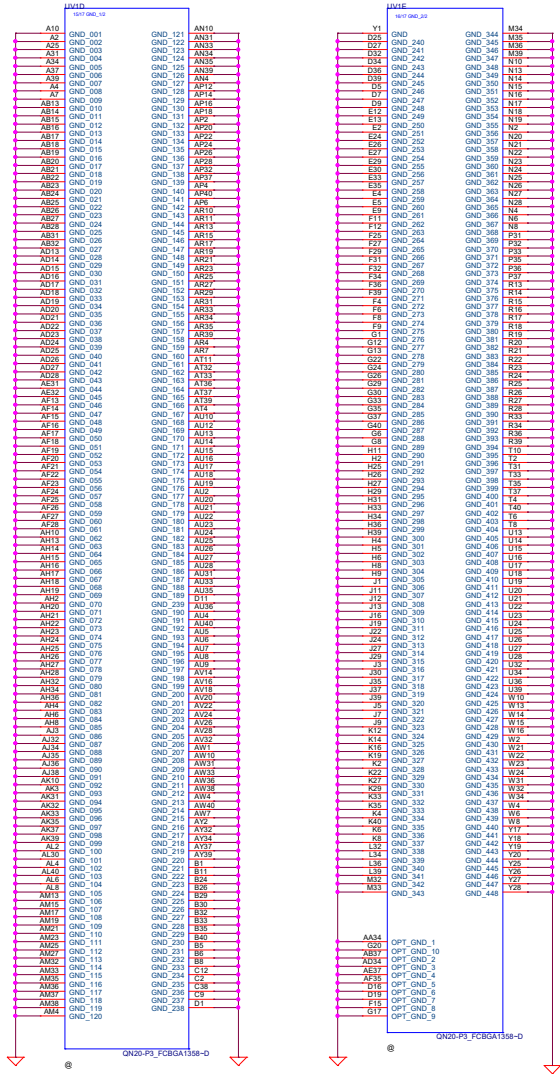
1UF_0402 X 12 pcs
10UF_0603 X 4 pcs

Place near GPU

22UF_0603 X 5 pcs
10UF_0603 X 2 pcs

GPU	Capacitor Type	Footprint	Population		Location	
			GB5-128	GB5B-128		
FBVDD/Q Supply Rail						
GB5-128	1 μ F	X6S	0402 or 0201W	12	12	Under GPU
GB5B-128	10 μ F	X6S	0603	4	4	Under GPU
	10 μ F	X6S	0603	2	2	Near GPU
	22 μ F	X6S	0603W	5	5	Near GPU

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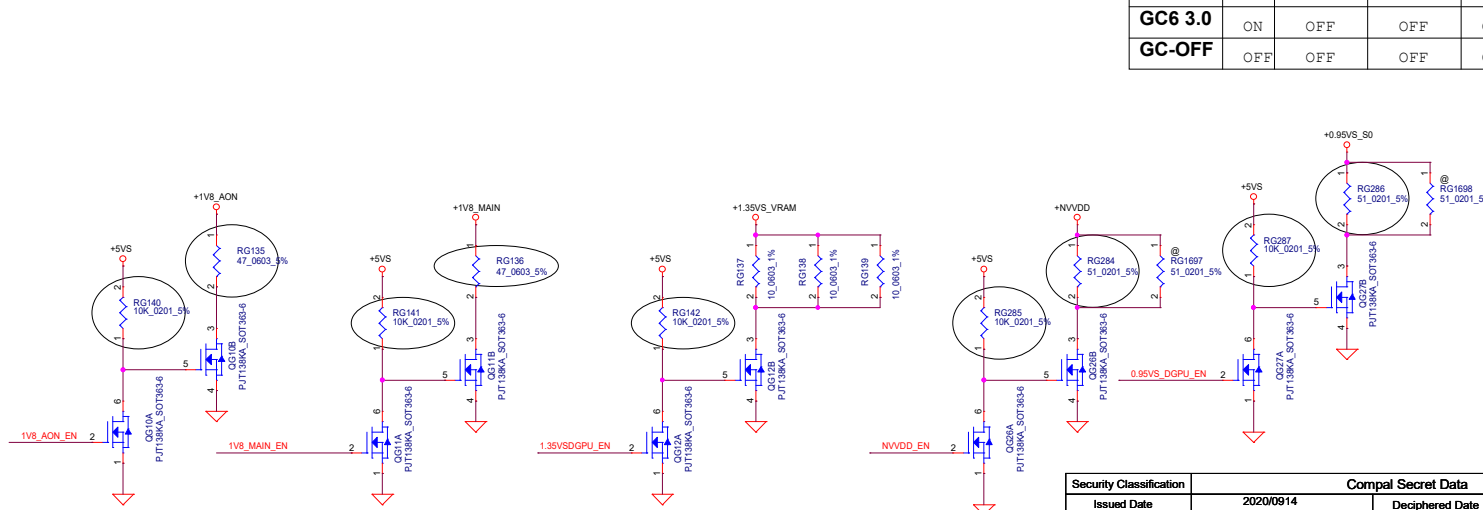
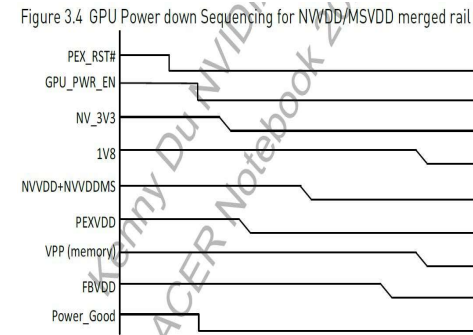
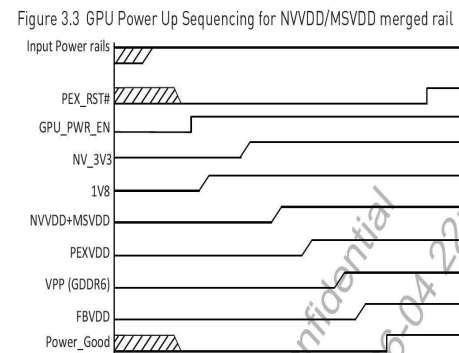
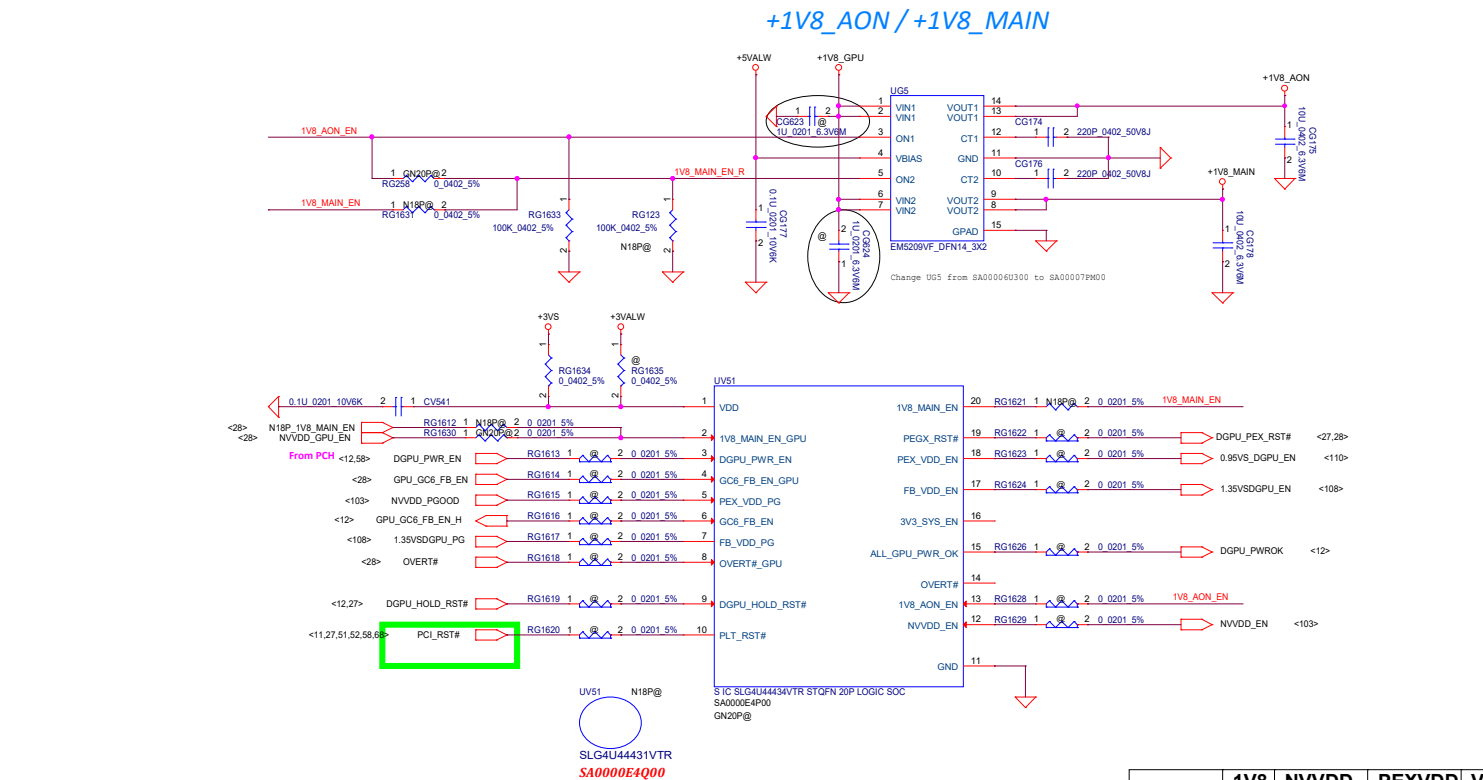
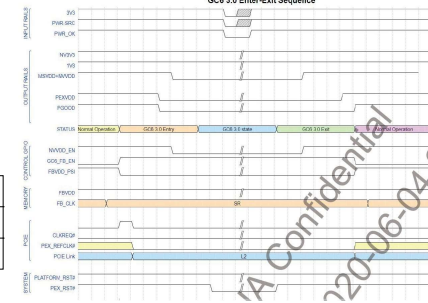
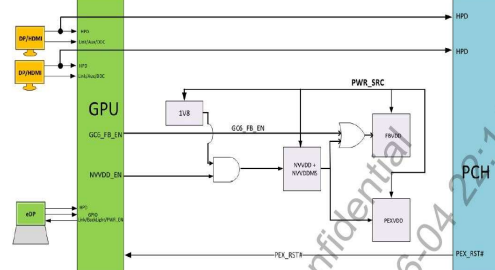


Figure 4.10 GC6 3.0 Entry and Exit Detailed Timing



	1V8	NVDD	PEXVDD	VPP	FBVDD
GC6 3.0	ON	OFF	OFF	ON	ON
GC-OFF	OFF	OFF	OFF	OFF	OFF

Figure 4.8 GC6 3.0 Block Diagram



Power Monitor(OVR-M)

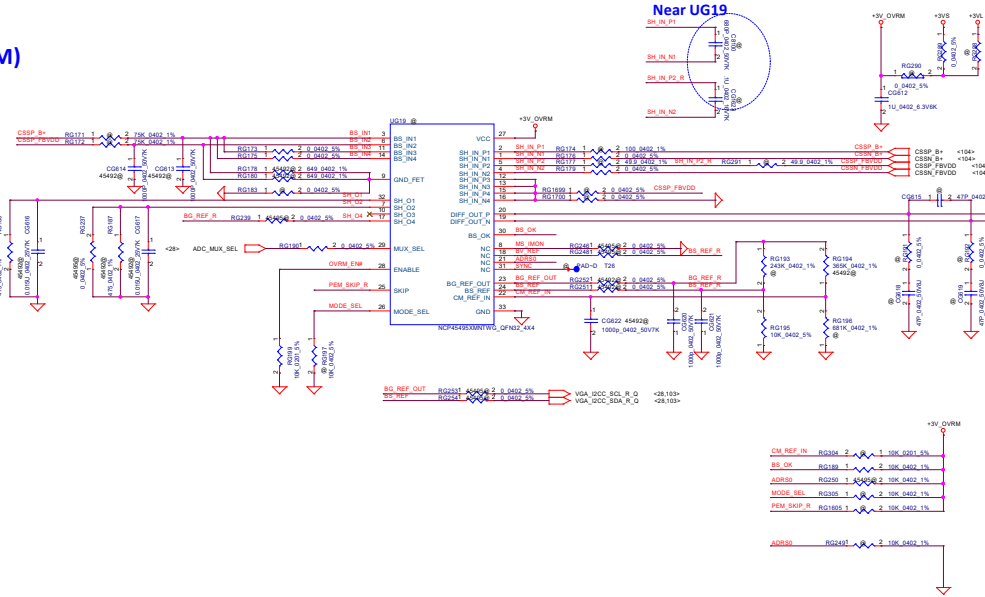
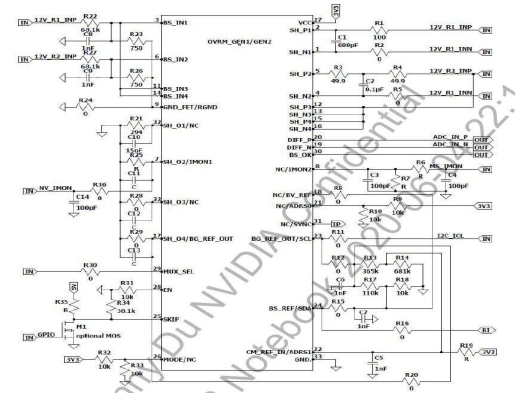


Figure 3.5 OVR-M GEN1 and GEN2 Co-Design



OVR-M Gen2 (Only For GN20)

UC19 45495	R0171 45495	R0172 45495	R0174 45495	R0177 45495	R0251 45495	R0198 45495	R0193 45495	C0153 45495	R0183 45495	R0189 45495	C0155 45495	R0185 45495
NCP45485	0.0402_5%	0.0402_5%	0.0402_5%	49.9_0402_1%	49.9_0402_1%	10K_0402_5%	31.6K_0402_1%	.1U_0402_16V7K	0.0402_5%	0.0402_5%	680P_0402_50V7K	10K_0402_5%
SA00000000	SD03479280	SD03479280	SD034499A0	SD034499A0	SD034499A0	SD034499A0	SD034499A0	SE07104K80	SD02800080	SD02800080	SE07481K80	SD02810280

OVR-M Gen1 (Onsemi) (N18P-G61A)

UC19 45492	R0171 45492	R0172 45492	R0174 45492	R0177 45492	R0251 45492	R0198 45492	R0193 45492	C0153 45492	R0183 45492	R0189 45492	C0155 45492	R0185 45492
NCP45482	75K_0402_1%	75K_0402_1%	100_0402_1%	49.9_0402_1%	49.9_0402_1%	681K_0402_1%	243K_0402_1%	.1U_0402_16V7K	0.0402_5%	0.0402_5%	680P_0402_50V7K	10K_0402_5%
SA00000000	SD03479280	SD03479280	SD03410080	SD034499A0	SD034499A0	SD03481380	SD03000420	SE07104K80	SD02800080	SD02800080	SE07481K80	SD02810280

OVR-M Gen1 (UPI) (N18P-G61A)

UC19 UPI	R0171 UPI	R0172 UPI	R0174 UPI	R0177 UPI	R0251 UPI	R0198 UPI	R0193 UPI	C0153 UPI	R0183 UPI	R0189 UPI	C0155 UPI	R0185 UPI
US0600Q0K1	75K_0402_1%	75K_0402_1%	100_0402_1%	49.9_0402_1%	49.9_0402_1%	681K_0402_1%	243K_0402_1%	.1U_0402_16V7K	0.0402_5%	0.0402_5%	680P_0402_50V7K	10K_0402_5%
SA00000000	SD03479280	SD03479280	SD03410080	SD034499A0	SD034499A0	SD03481380	SD03000420	SE07104K80	SD02800080	SD02800080	SE07481K80	SD02810280

OVR-M Gen1 (Onsemi) (GN20) (Reserve Only)

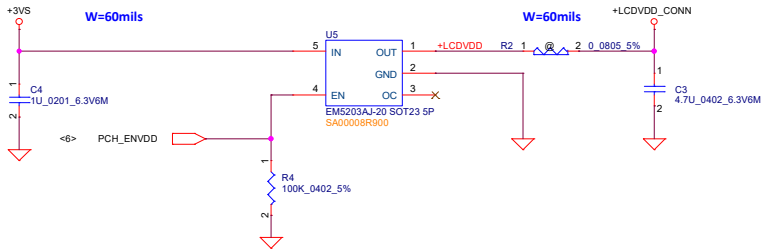
UC19 45492	45492_FuGN20Gent1	45492_FuGN20Gent1	45492_FuGN20Gent1	45492_FuGN20Gent1	45492_FuGN20Gent1	45492_FuGN20Gent1	45492_FuGN20Gent1	45492_FuGN20Gent1	45492_FuGN20Gent1	45492_FuGN20Gent1	45492_FuGN20Gent1	45492_FuGN20Gent1
NCP45482	75K_0402_1%	75K_0402_1%	100_0402_1%	49.9_0402_1%	49.9_0402_1%	681K_0402_1%	237K_0402_1%	.1U_0402_16V7K	0.0402_5%	0.0402_5%	680P_0402_50V7K	10K_0402_5%
SA00000000	SD03479280	SD03479280	SD03410080	SD034499A0	SD034499A0	SD03481380	SD03000420	SE07104K80	SD02800080	SD02800080	SE07481K80	SD02810280

OVR-M Gen1 (UPI) (GN20) (Reserve Only)

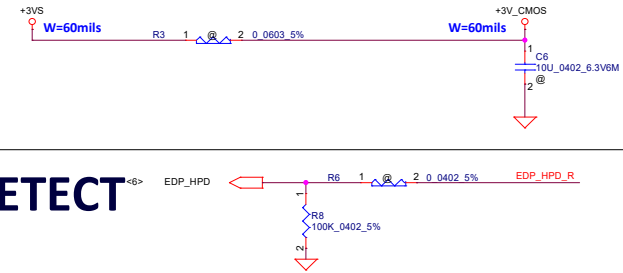
UC19 UPI	UPI_FuGN20Gent1	UPI_FuGN20Gent1	UPI_FuGN20Gent1	UPI_FuGN20Gent1	UPI_FuGN20Gent1	UPI_FuGN20Gent1	UPI_FuGN20Gent1	UPI_FuGN20Gent1	UPI_FuGN20Gent1	UPI_FuGN20Gent1	UPI_FuGN20Gent1	UPI_FuGN20Gent1
US0600Q0K1	75K_0402_1%	75K_0402_1%	100_0402_1%	49.9_0402_1%	49.9_0402_1%	681K_0402_1%	316K_0402_1%	.1U_0402_16V7K	0.0402_5%	0.0402_5%	680P_0402_50V7K	10K_0402_5%
SA00000000	SD03479280	SD03479280	SD03410080	SD034499A0	SD034499A0	SD03481380	SD03000420	SE07104K80	SD02800080	SD02800080	SE07481K80	SD02810280

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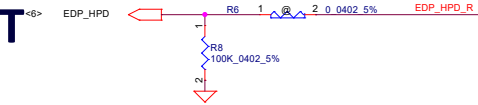
LCD POWER SWITCH



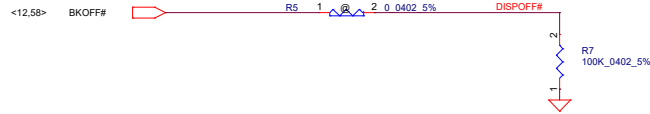
IR CAMERA POWER CIRCUIT



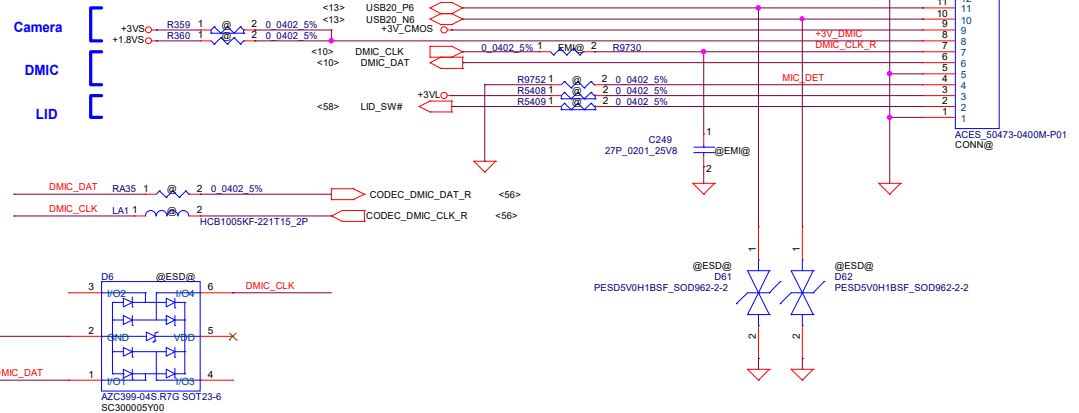
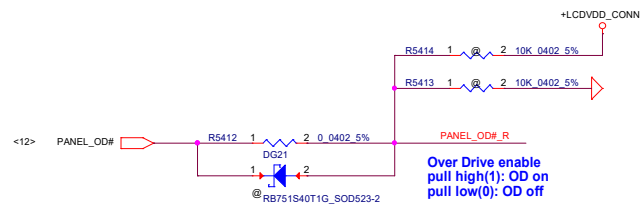
HOT PLUG DETECT



DISPLAY OFF



eDP CONNECTOR



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Issued Date				Deciphered Date				eDP / Camera / Touch			
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B				B
A				A
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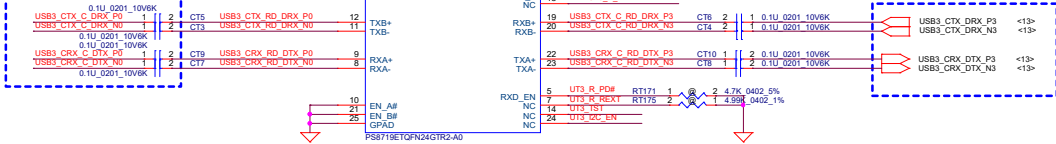
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C				C
B				B
A				A
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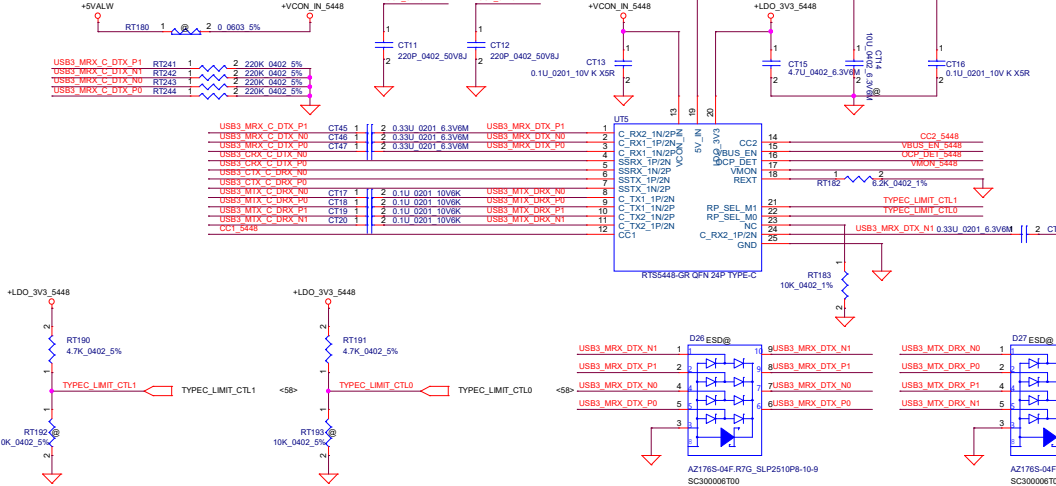
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USB3.1 Re-Driver

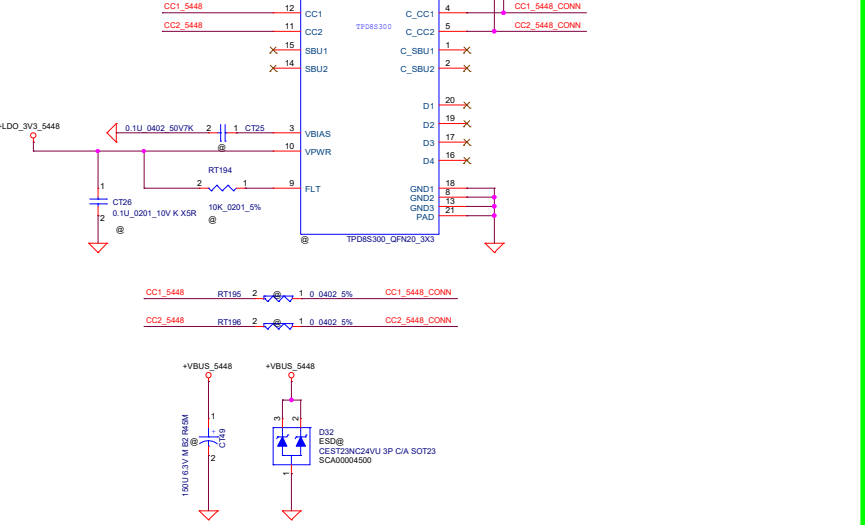
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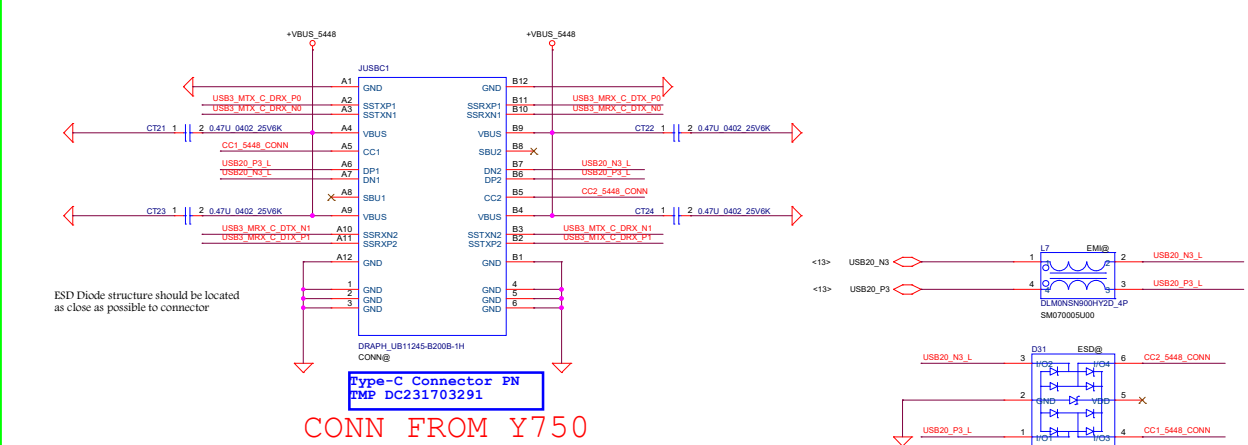
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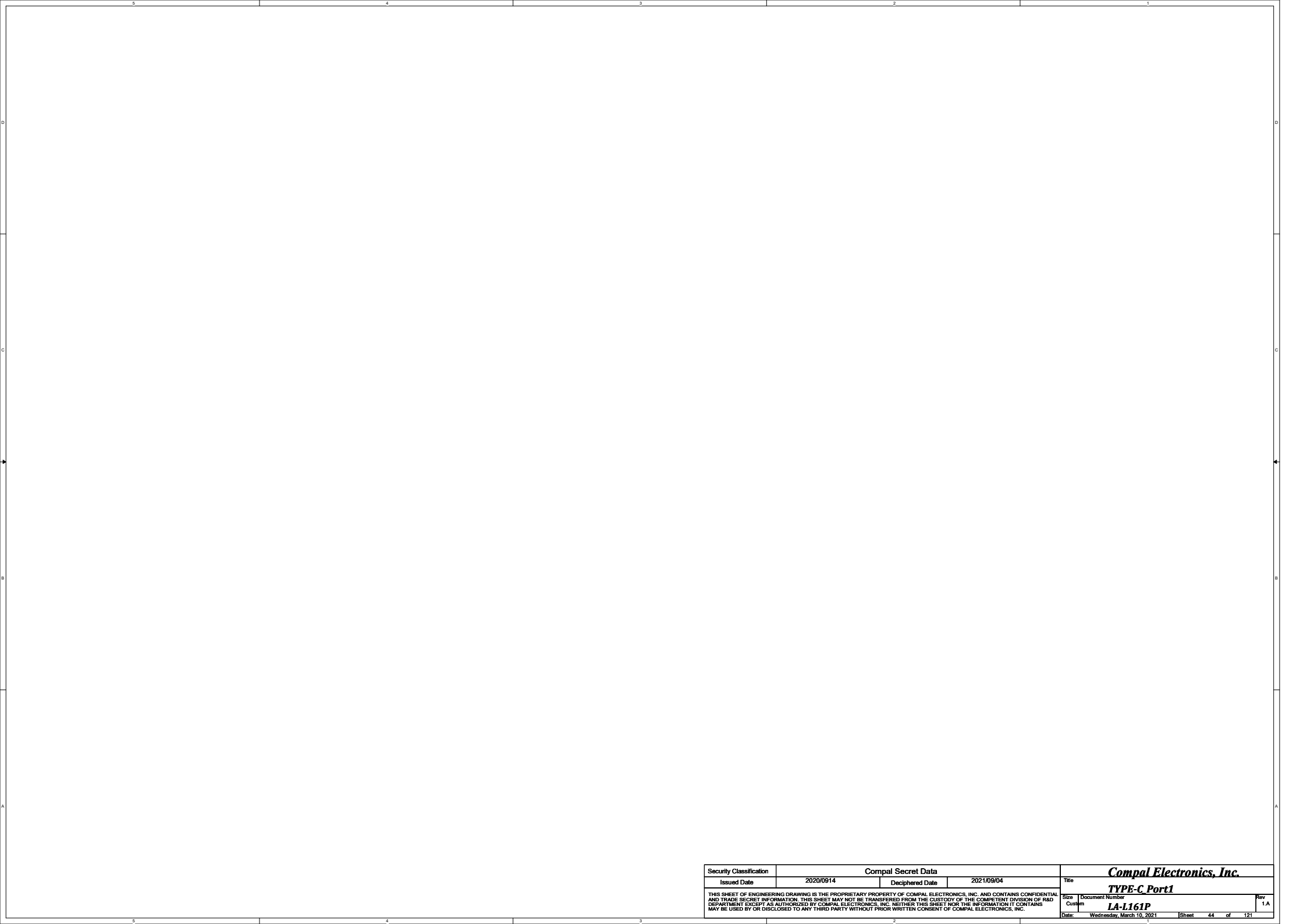


Type-C CONN

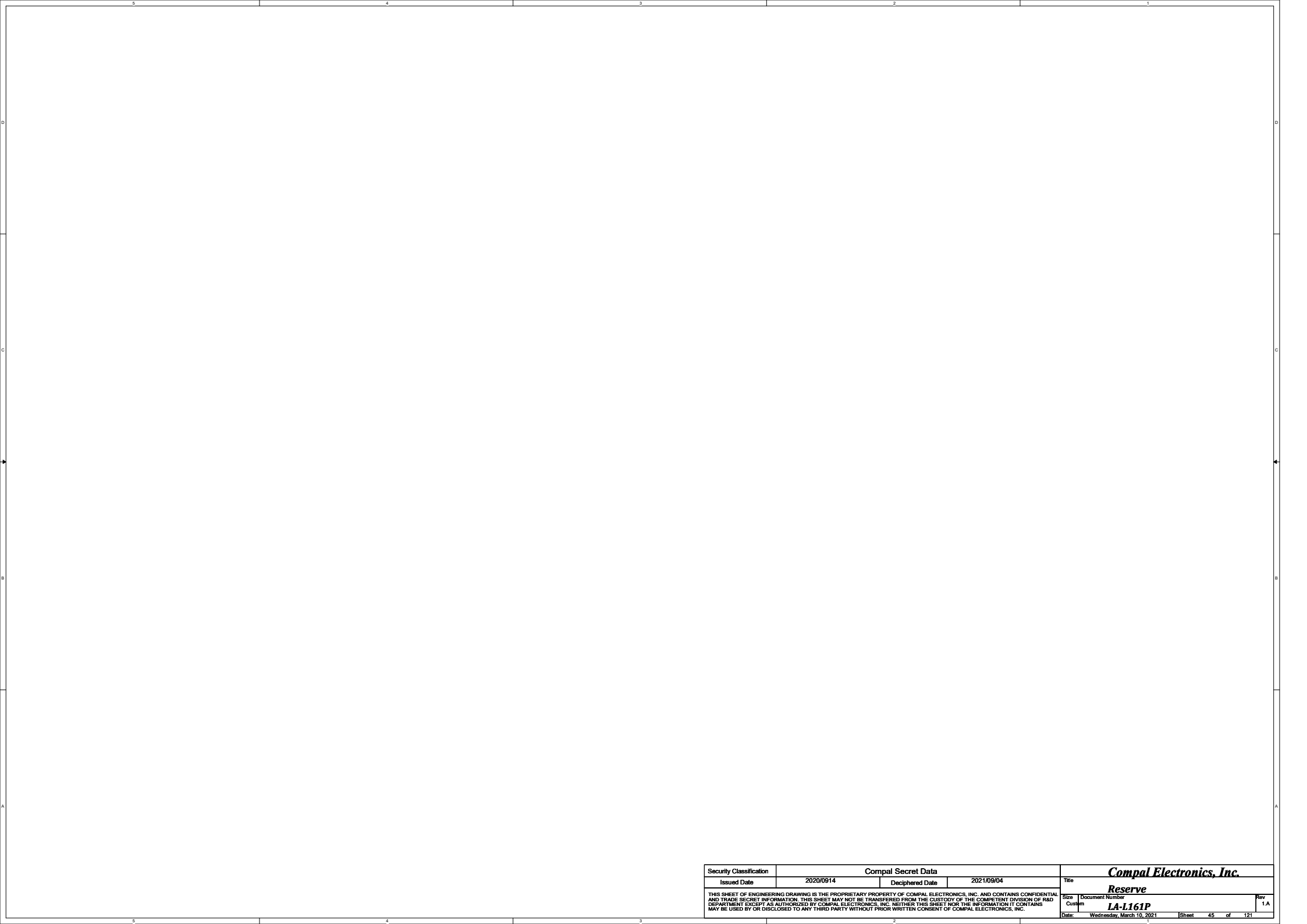


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A				A
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Issued Date	2020/0914	Deciphered Date	2021/09/04	TYPE-C Port1	
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B				B
A				A
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B				B
A				A
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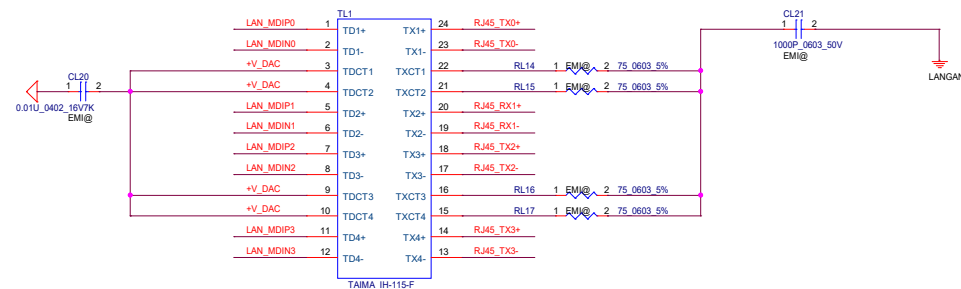
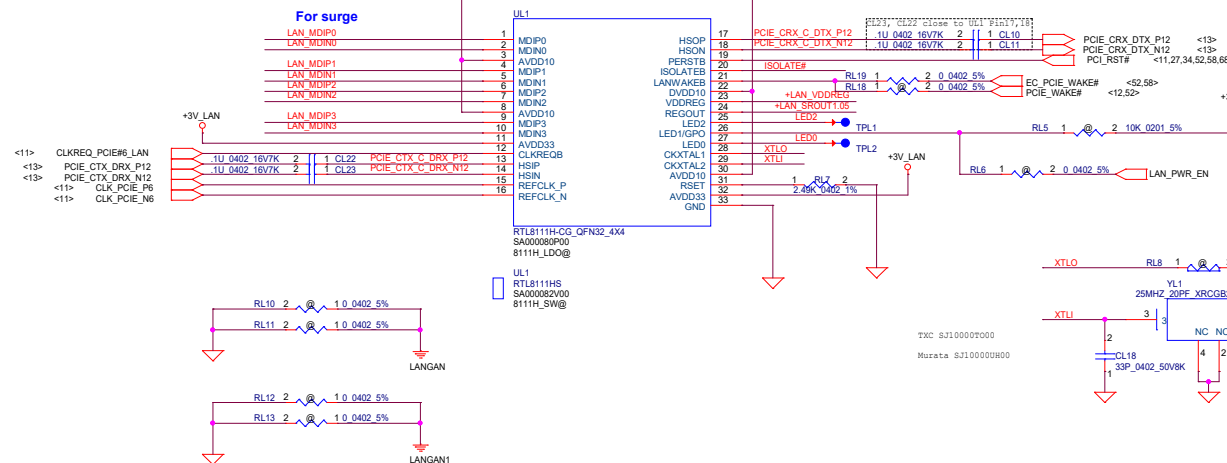
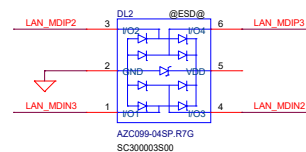
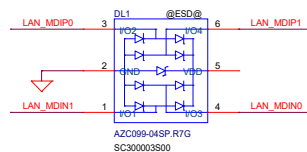
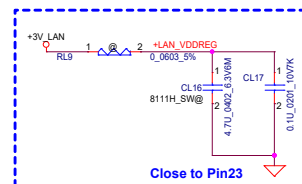
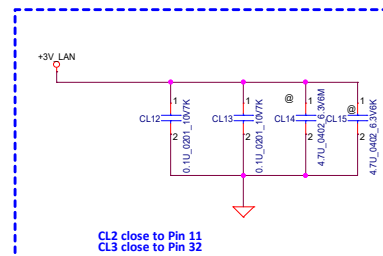
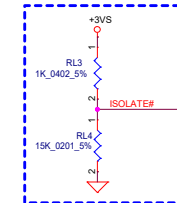
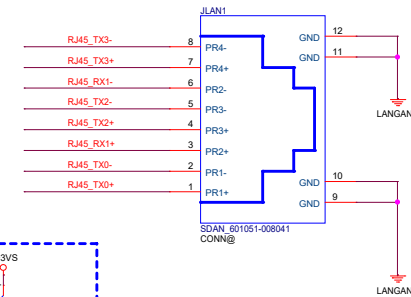
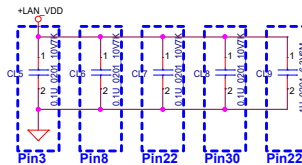
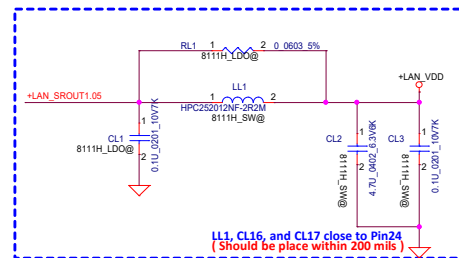
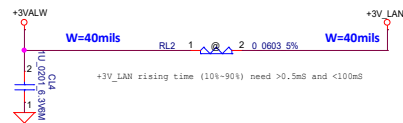
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B				B
A				A
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				Size Custom	Document Number LA-L161P
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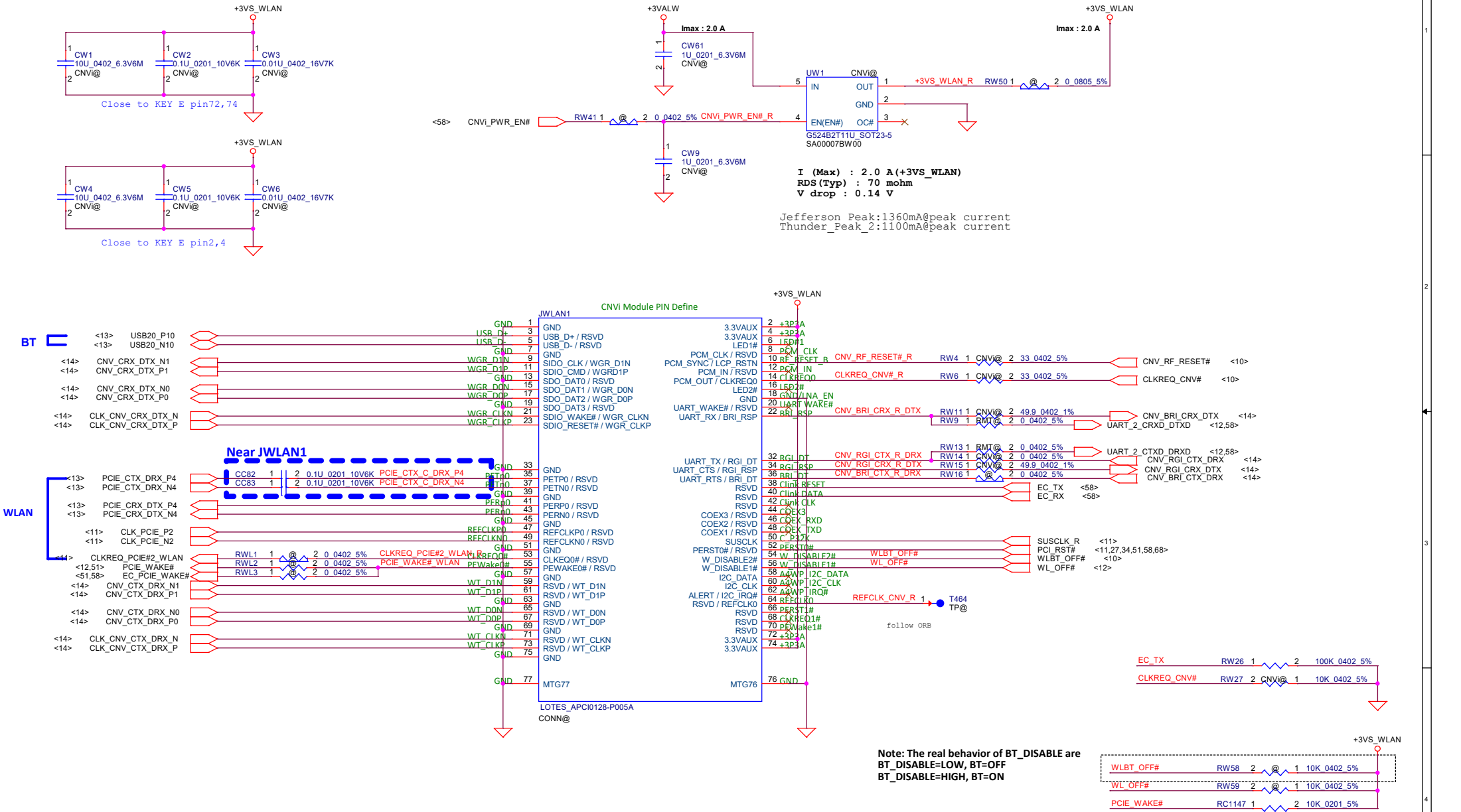
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NGFF WLAN / BT (Key E)

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

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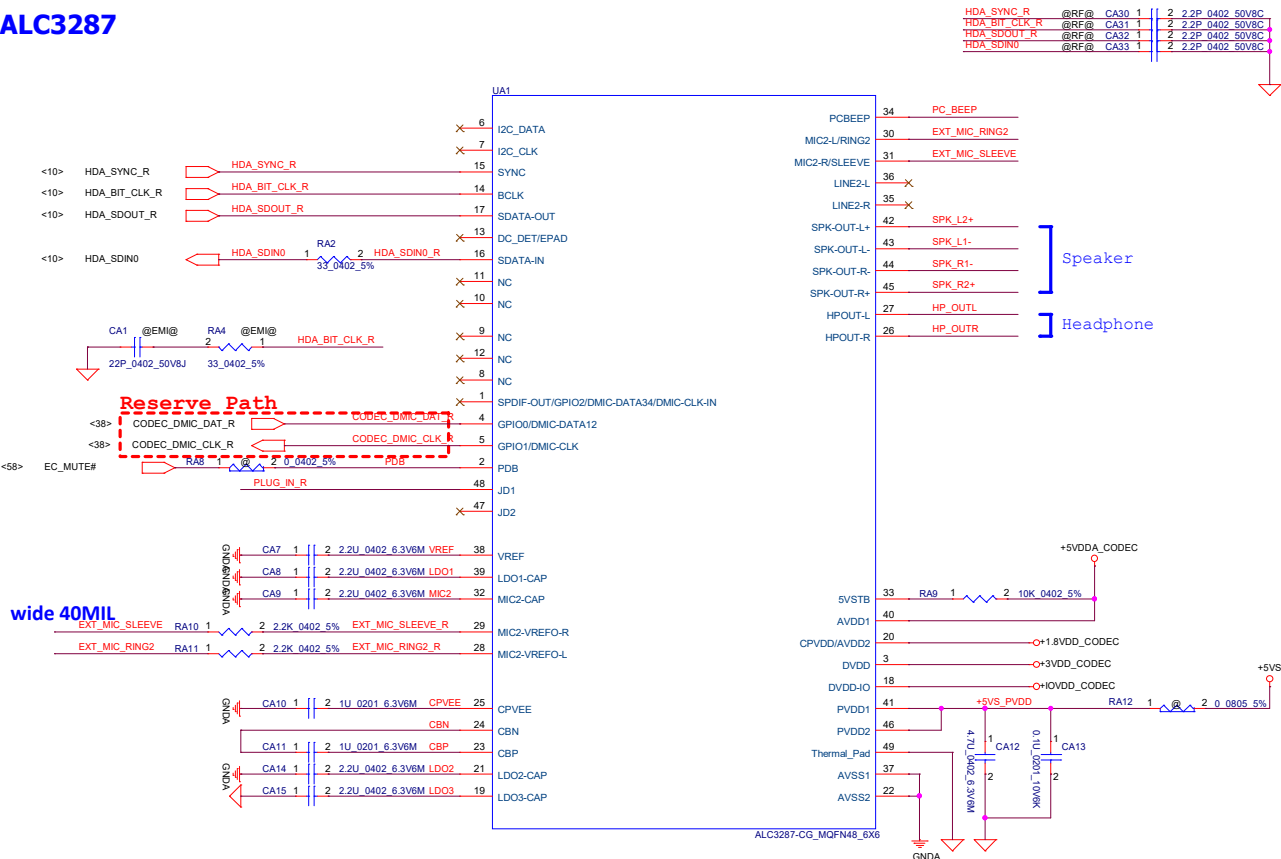
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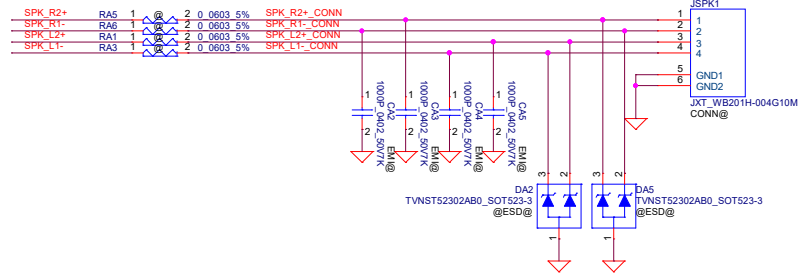
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ALC3287



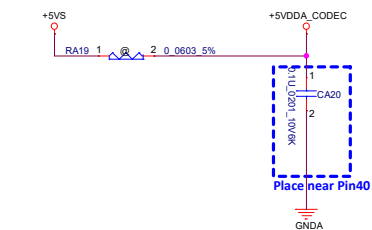
Speaker

SPEAK 4 ohm : 40MIL
SPEAK 8 ohm : 20MIL

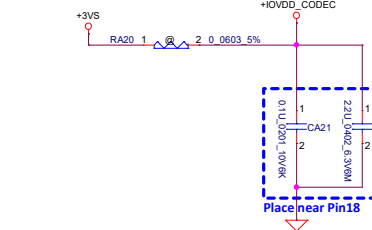


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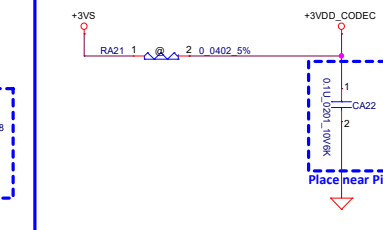
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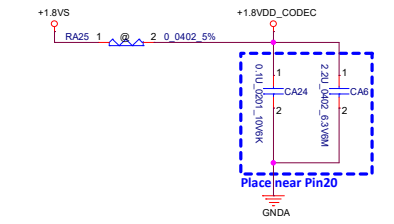
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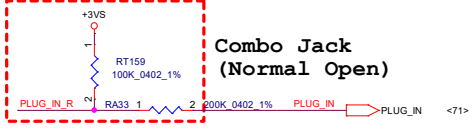
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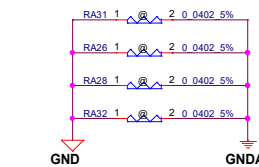
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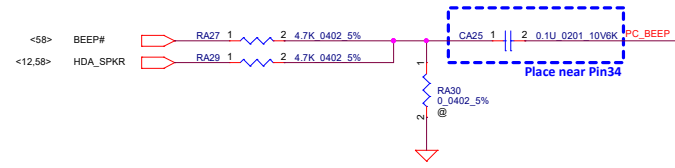
Close Audio codec



Combo Jack
(Normal Open)



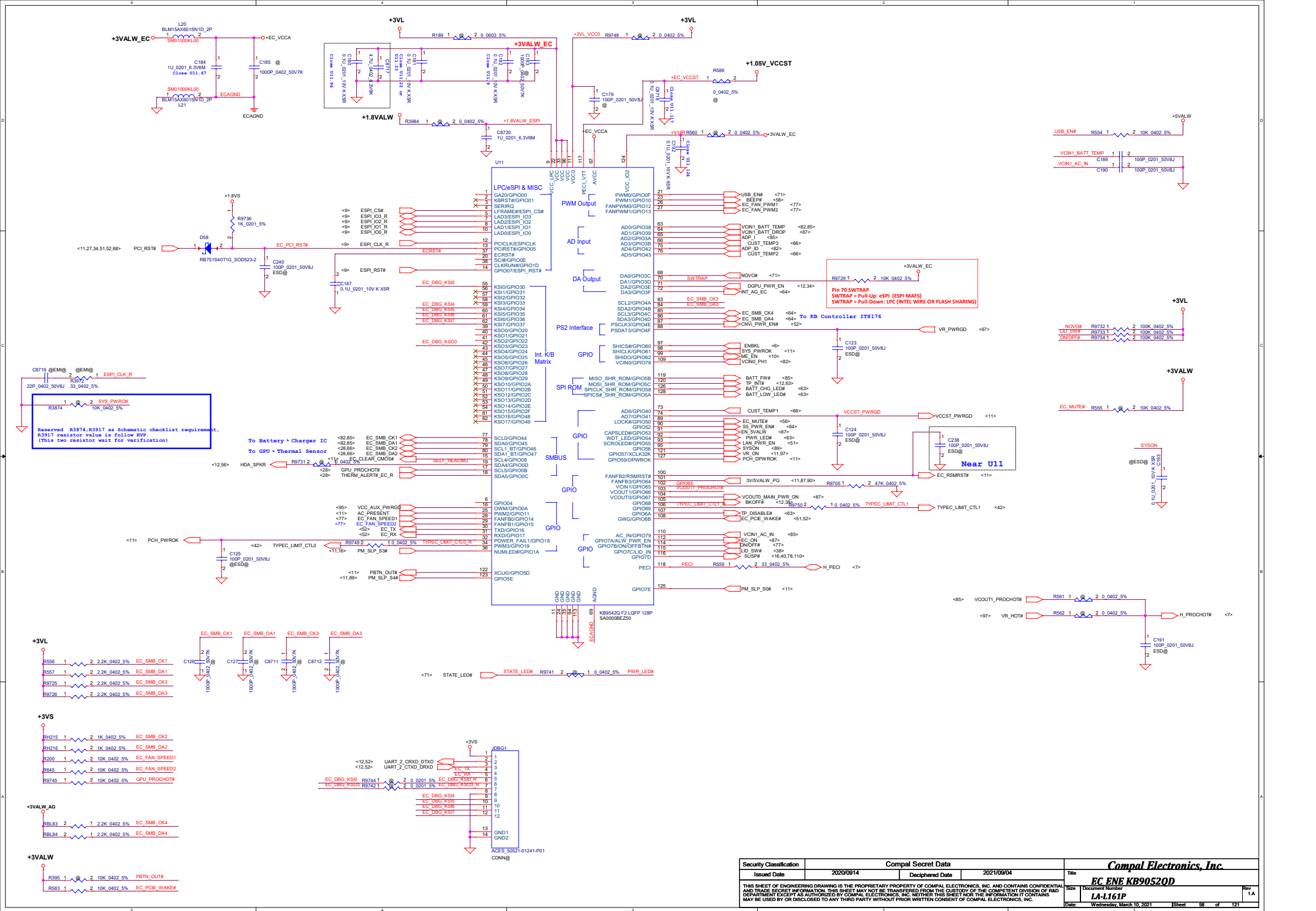
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2020/09/14		2021/09/04		1A		LA-L161P	
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B				B
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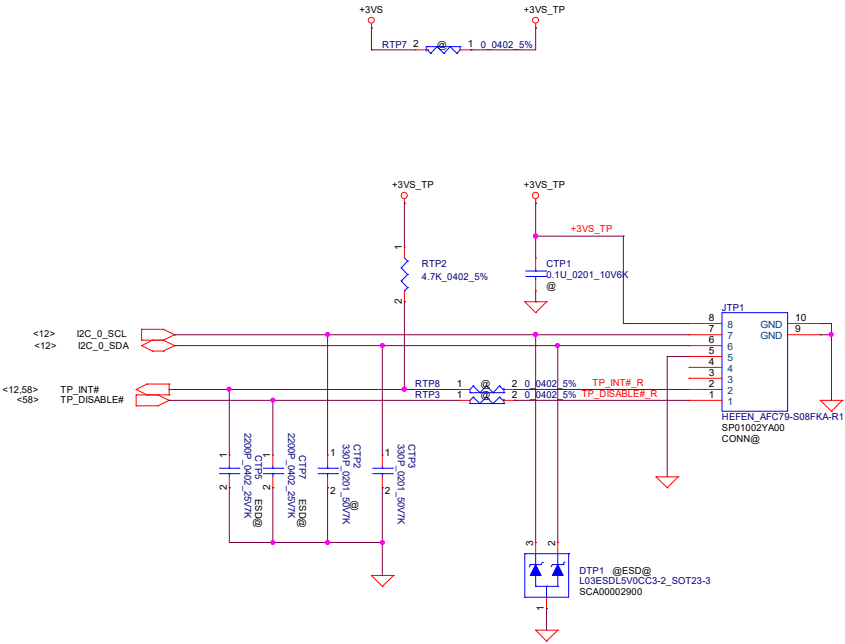
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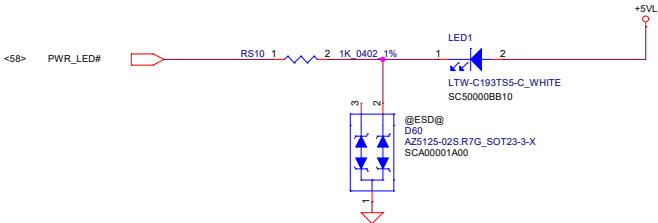
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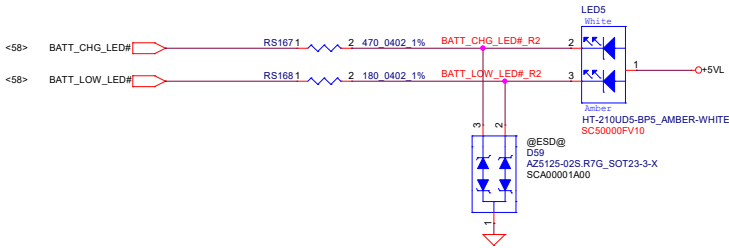
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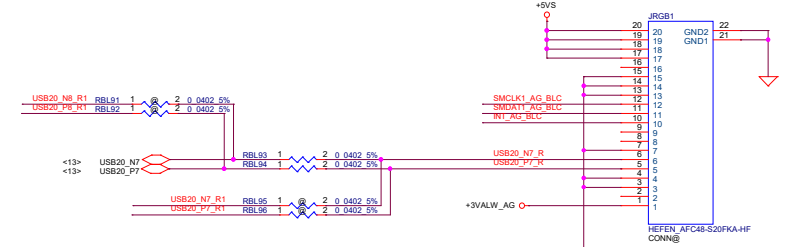
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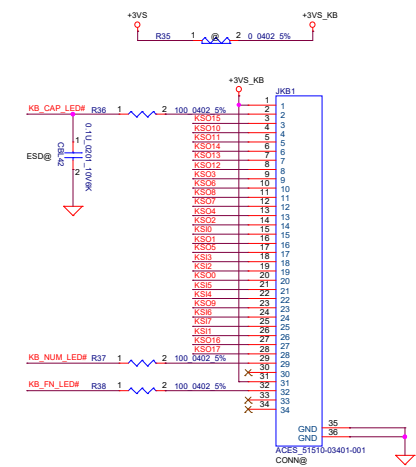
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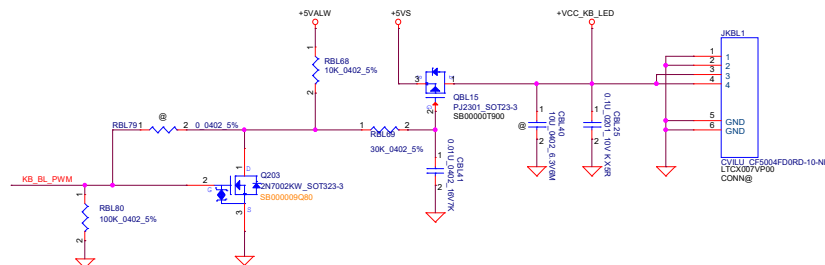
Keyboard RGB Backlight



Keyboard



Keyboard White Backlight



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Size	Custom	Document Number	LA-L161P	Rev 1A
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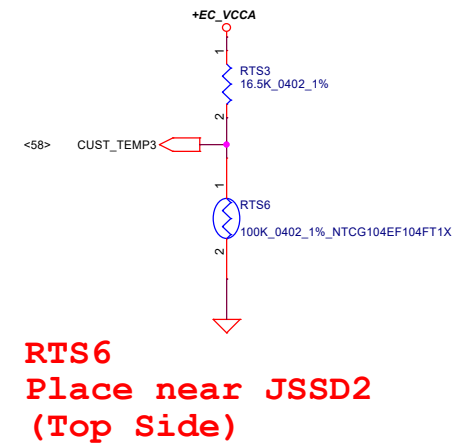
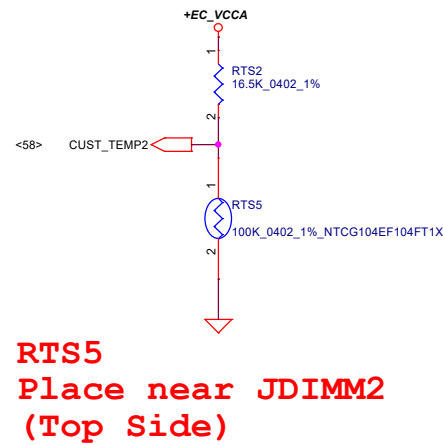
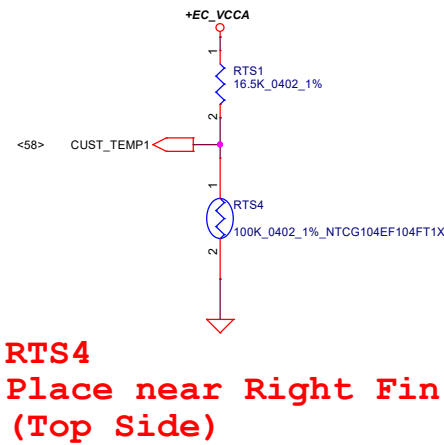
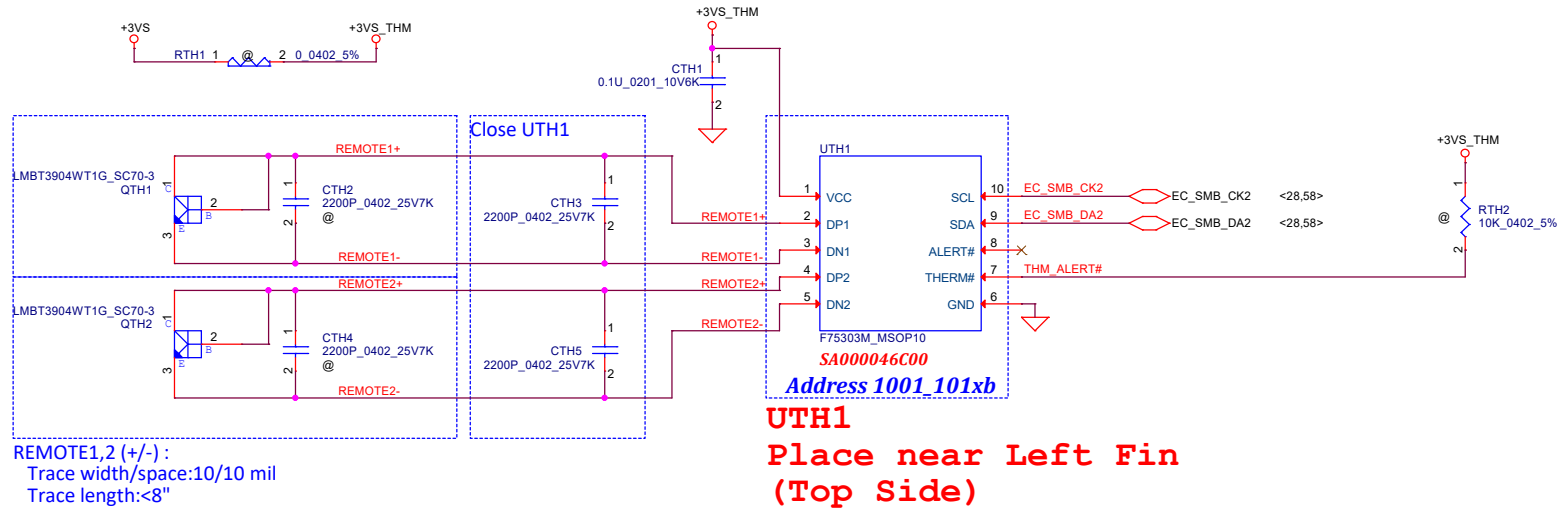
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THERMAL SENSOR

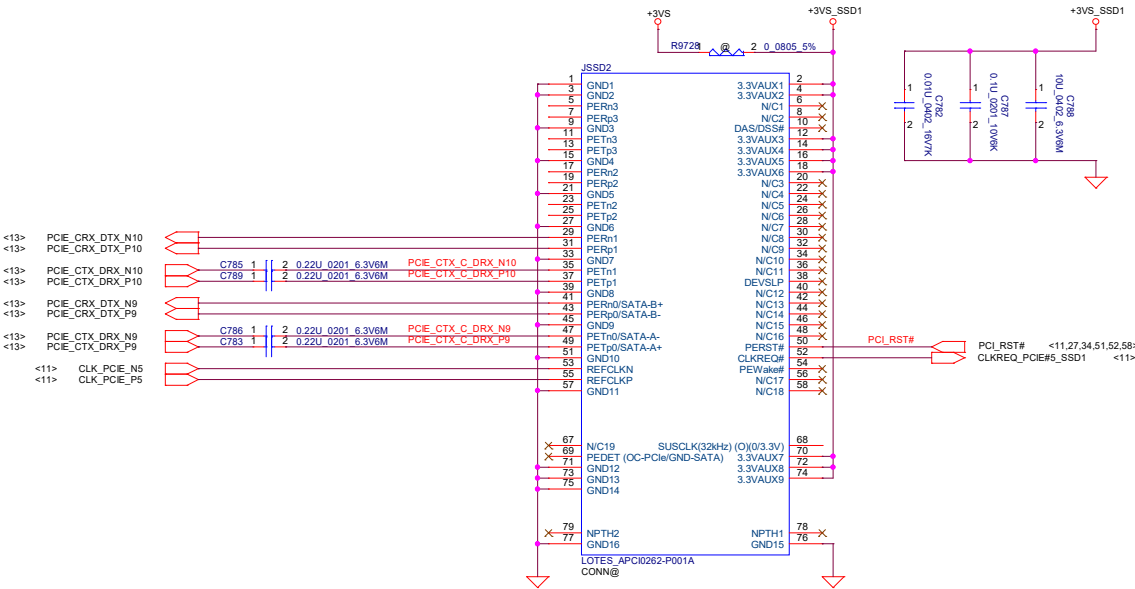
QTH1
Place near +NVVDD
(Bottom Side)

QTH2
Place near +VCCIN
(Bottom Side)

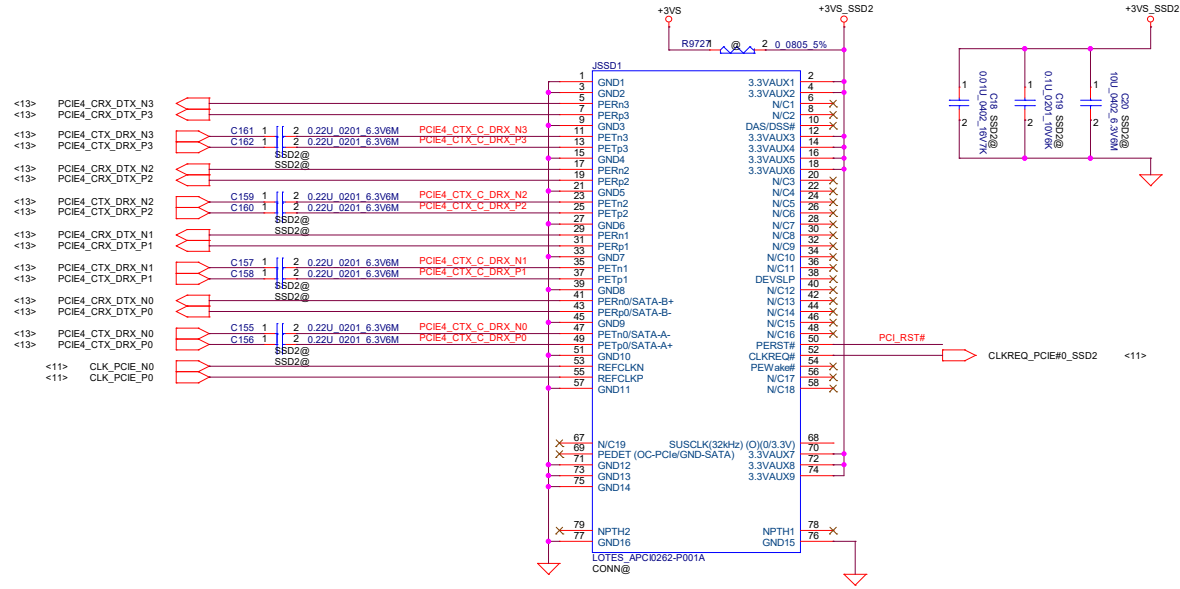


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SSD2_2280 (TYPE M) Second (PCIe Gen3)(Option)



SSD1_2242 (TYPE M) Main (PCIe Gen4)



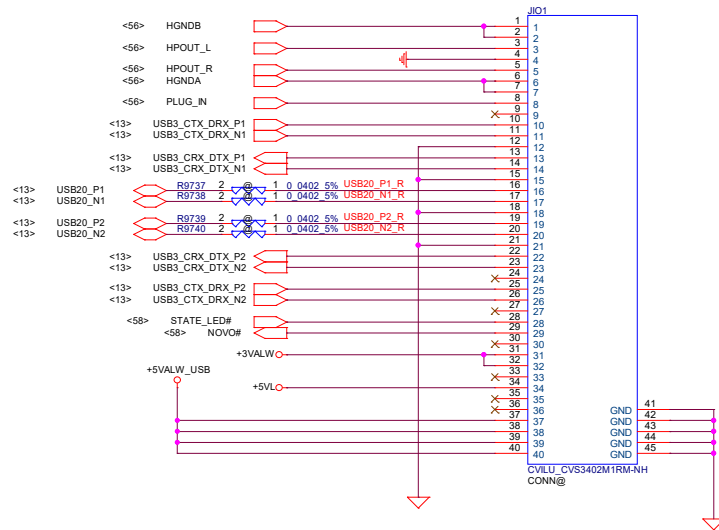
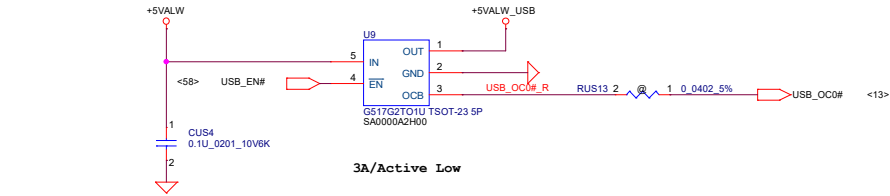
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IO connector



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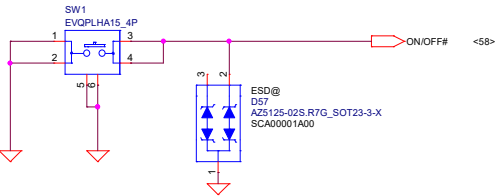
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				Size	Document Number
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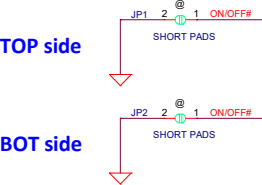
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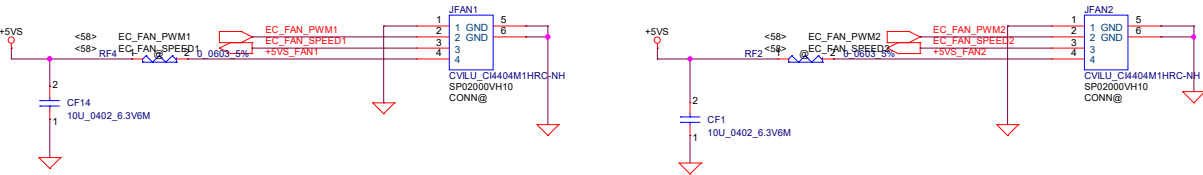
Power Button



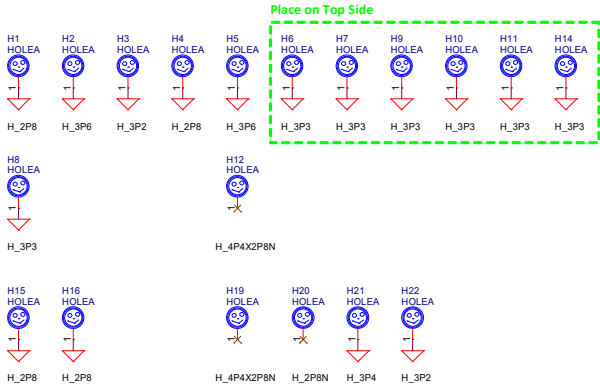
ON/OFF# SHORT PAD



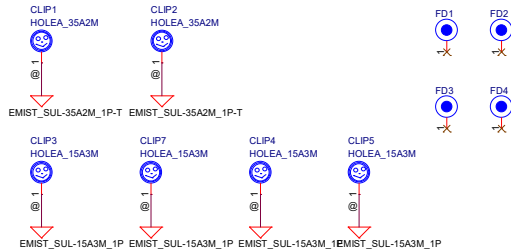
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SCREW

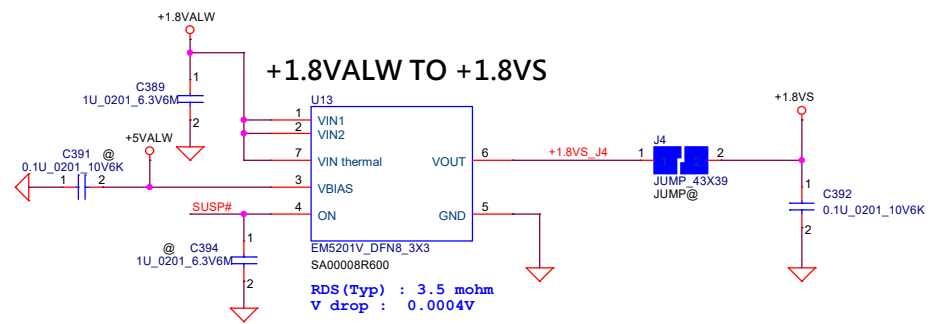
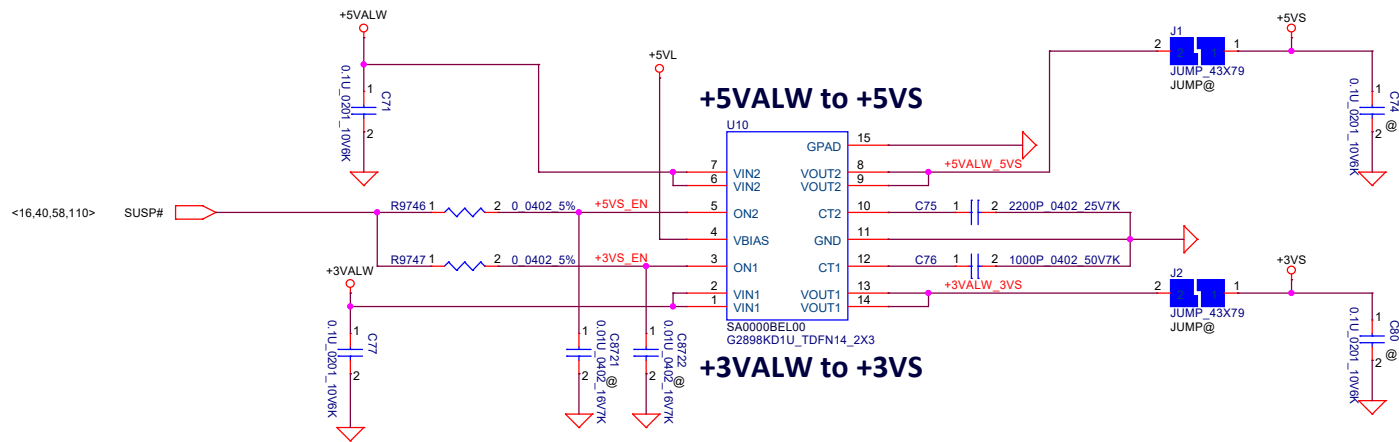


CLIP



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DC to DC



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								Size	Document Number	Rev
								Custom	LA-L161P	1.A
								Date:	Wednesday, March 10, 2021	Sheet

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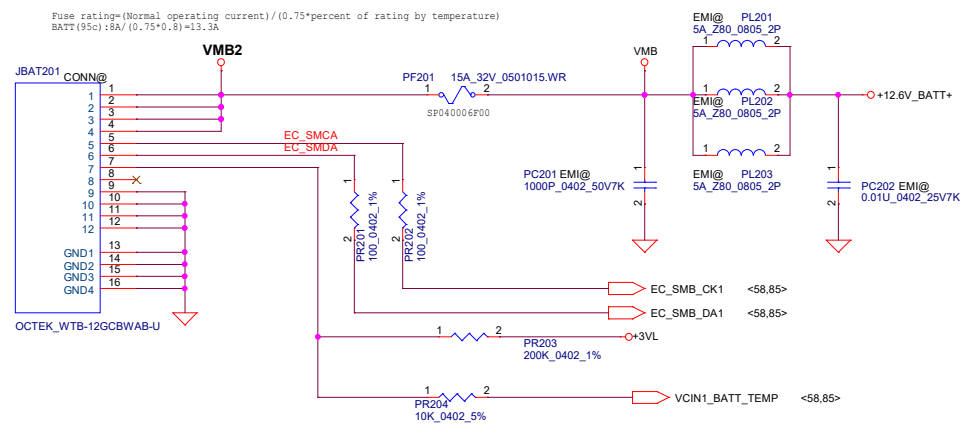
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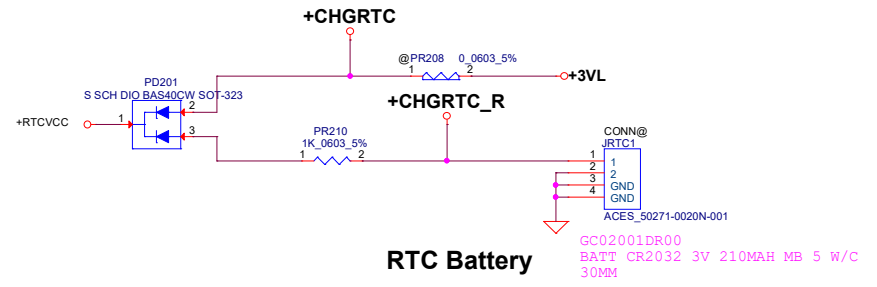
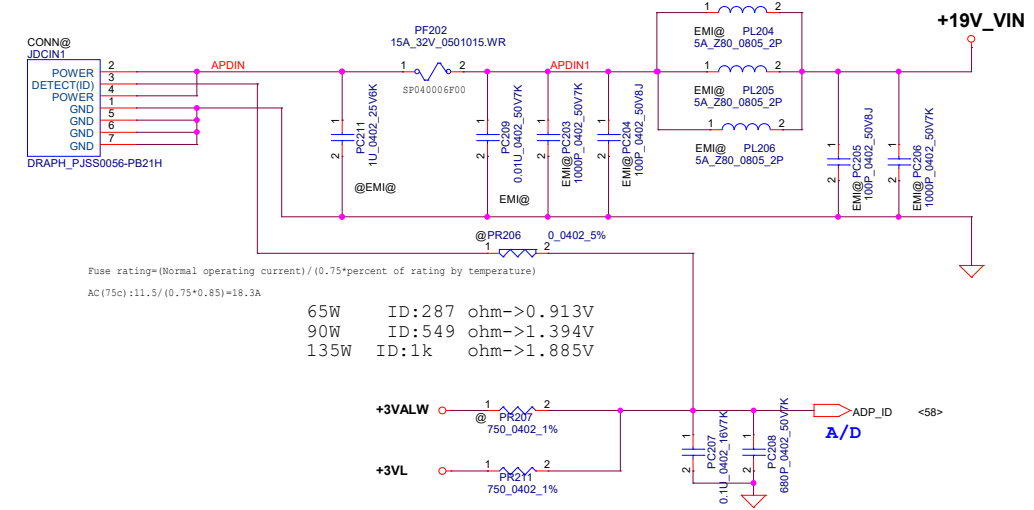
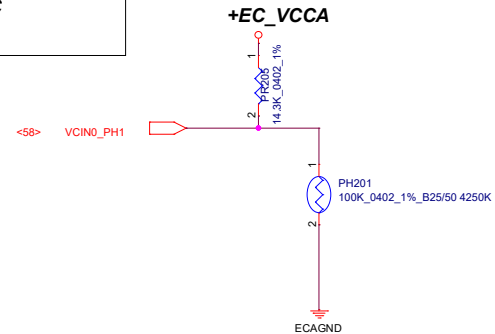
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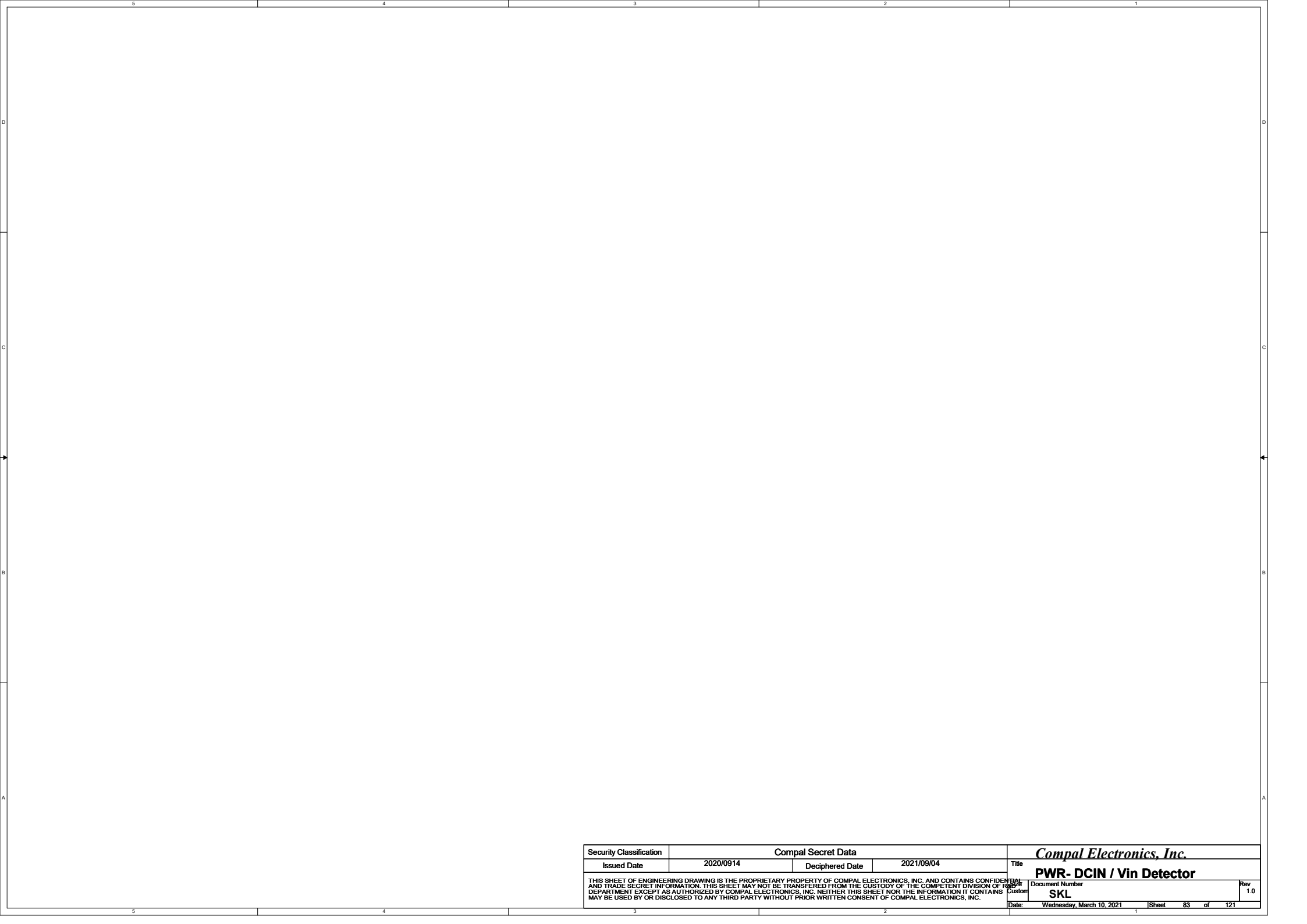
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PH201 under CPU botten side :
CPU thermal protection at 97 +3 degree C
Recovery at 59 +3 degree C

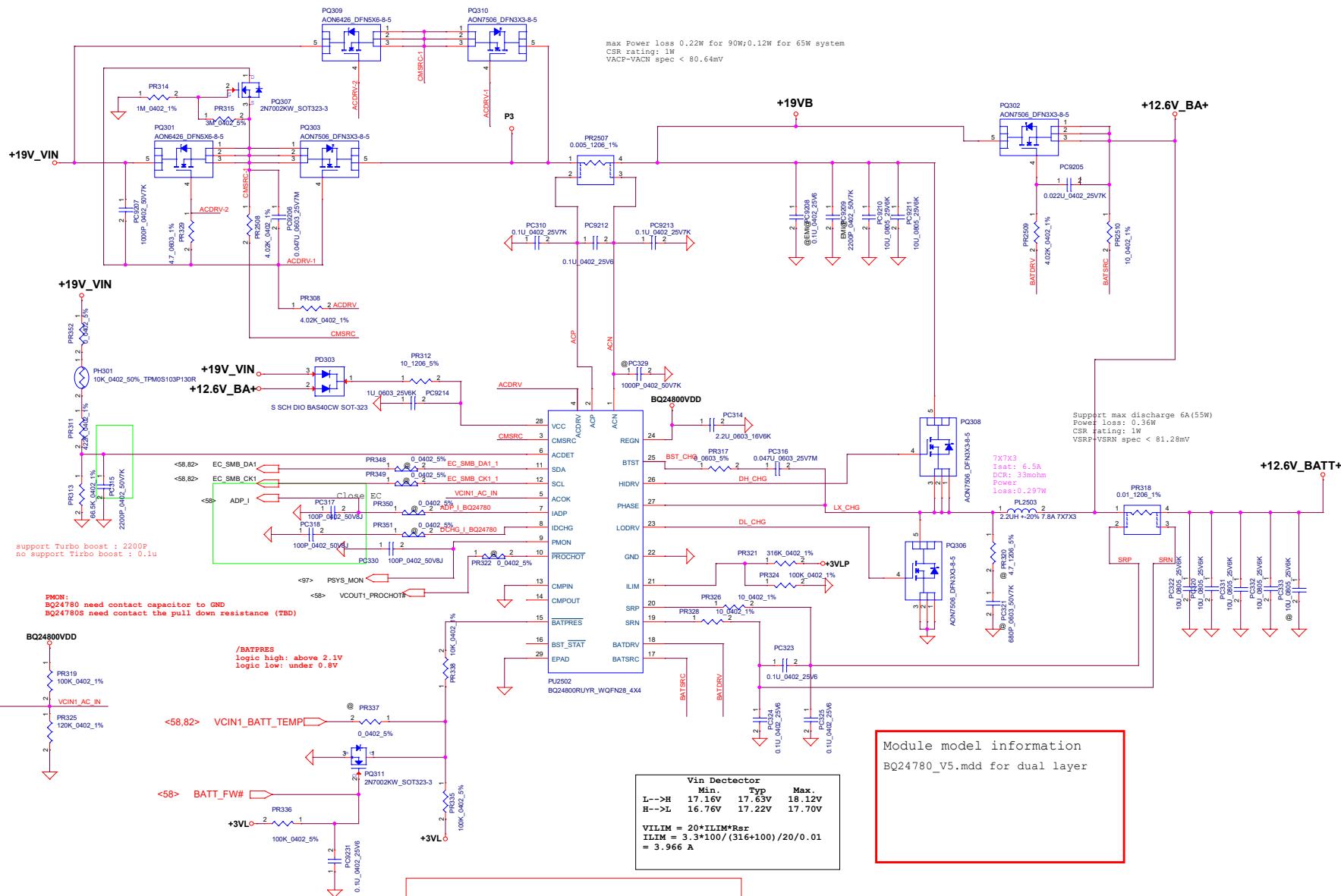




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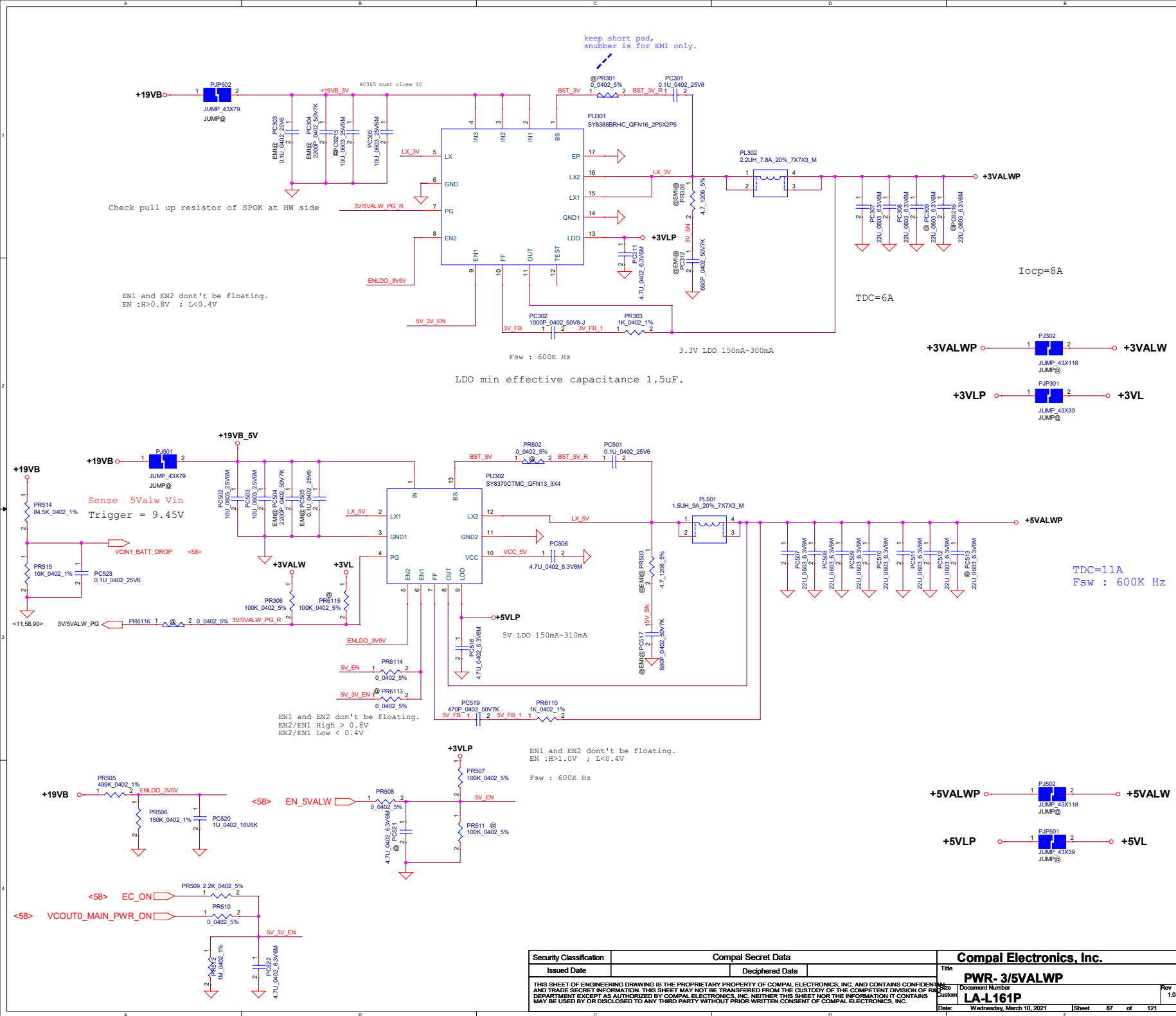
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PWR Reserve

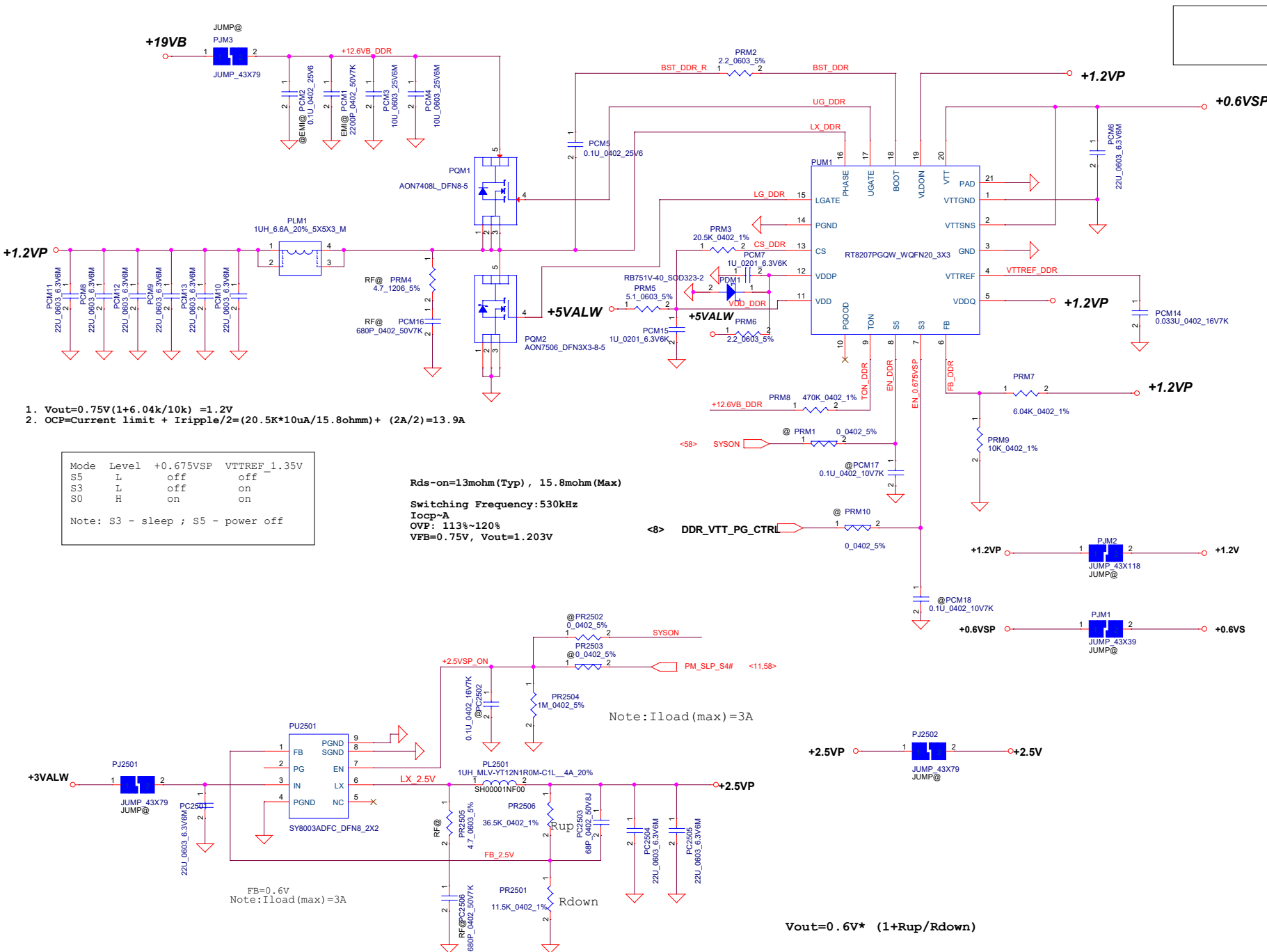
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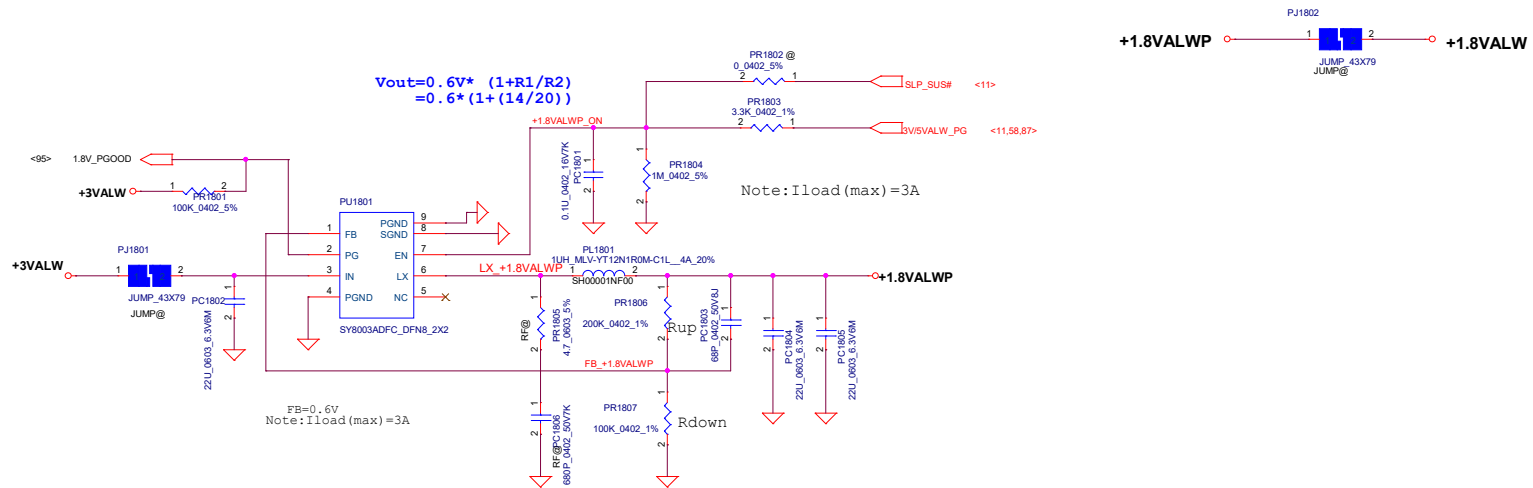
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Note:
 When design $V_{in} = 5V$, please stuff snubber
 to prevent V_{in} damage

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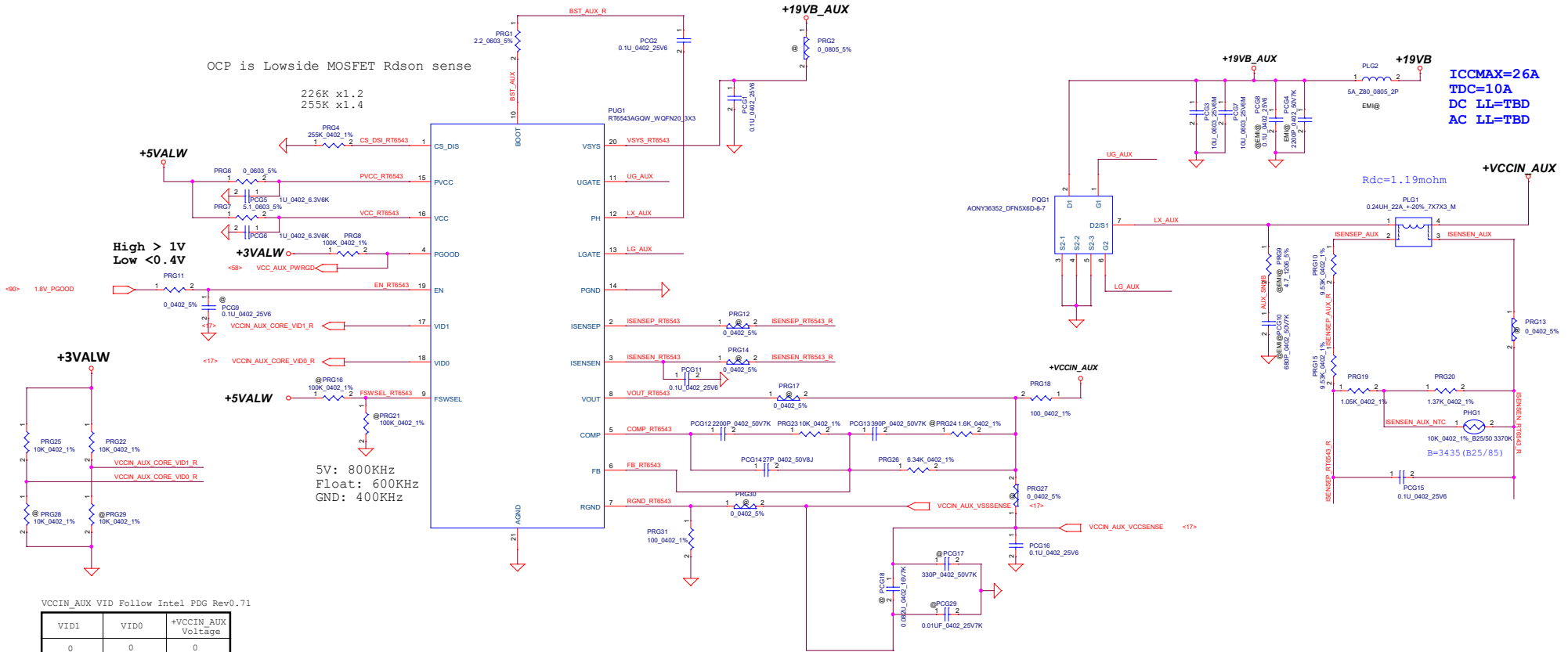
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Module model information
RT6543A_V1A.mdd for IC portion
RT6543A_V1B.mdd for SW portion

OCF is Lowside MOSFET Rds(on) sense

226K x1.2
255K x1.4



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Module model information

RT3613EE_3Phase_V1A.mdd for IC portion

RT3613EE_3Phase_V1B.mdd for SW portion

RT3613EEGQW-02 is not MP part

+5VALW

Pull High in HW site.

<58> VR_HOT#

VREF06_RT3613EE

0.6V

2 pahse
PRZ19 is 0ohm
PRZ27 is 7.68K ohm

VR_HOT# 100 degreeC
ALERT# 97 degreeC

+1.05V_VCCST

<15> SOC_SVID_CLK_R

<15> SOC_SVID_DAT_R

<15> SOC_SVID_ALERT#_R

+3VS

<58> VR_PWRGD

VREF06_RT3613EE

Close to Phasel Inductor

LL/130W Compensation

PHZ2 100K_0402_1% B25/50 4250K

NTC1P_VCCIN 1 2 NTC1N_VCCIN 1 2

PRZ55 16.9K_0402_1%

@ PCZ14 0.47U_0402_6.3V6K

PRZ50 16.2K_0402_1%

PRZ53 17.4K_0402_1%

PSYS_MON

IMON_RT3613EE

RT3613EEGQW-02_WQFN32_4X4

+19VB_VCCIN

High: > 0.7V
Low: < 0.3V

<98> 2 phase
PRZ75, PRZ76 are unpop.
PRZ68, PRZ70, PRZ71, PCZ82, PCZ83, PRZ72 unpop

ISEN1P

ISEN1N

ISEN2P

ISEN2N

ISEN3P

ISEN3N

NC

NC

NC

NC

NC

NC

VSEN

COMP

FB

RGND

GND

debug only

remote sense in HW site.

debug only

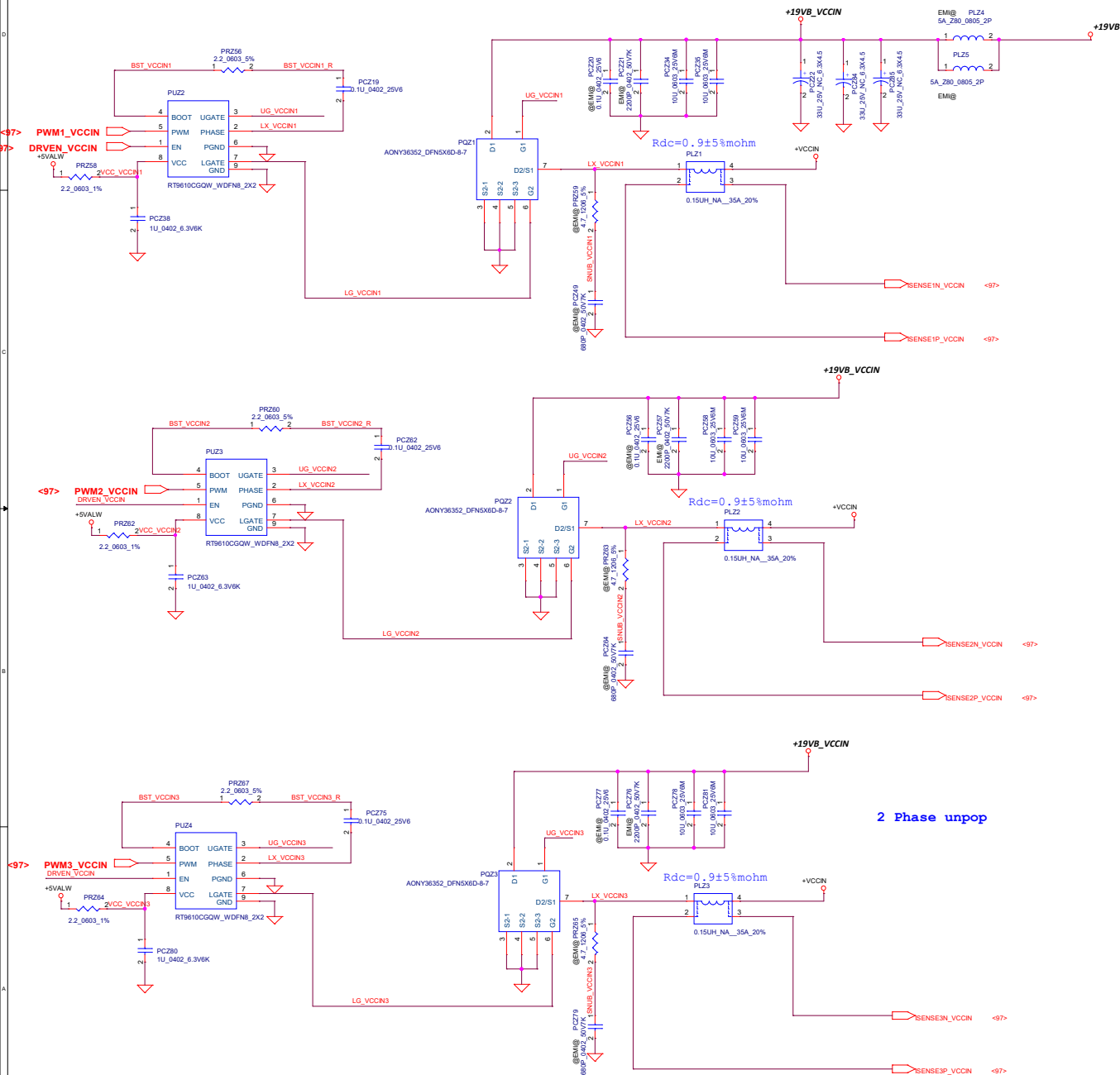
31 pin is a function to fix decay down slew rate to reduce acoustic noise.
High(5V): enable (5V is request)
Low:(0V): disable
this pin can dynamic change state.

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File	+VCCIN(RT3613EE)		
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ICCMAX=62A
TDC=36A

Frequency 600KHz



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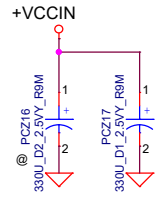
Compal Electronics			
CPU MOSMDecoupling cap			
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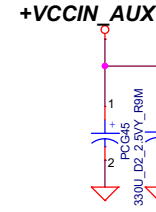
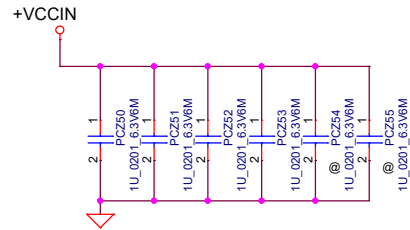
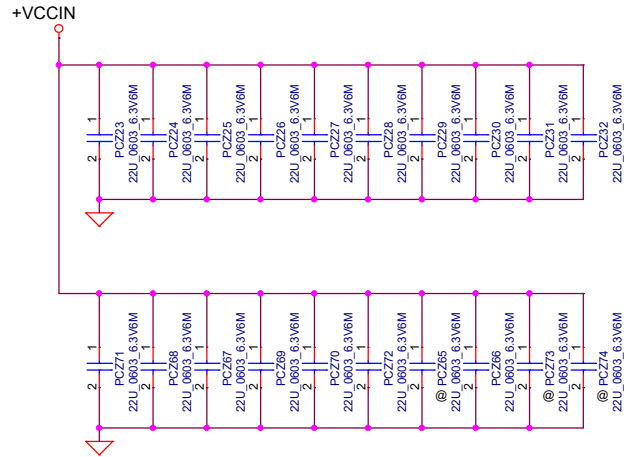
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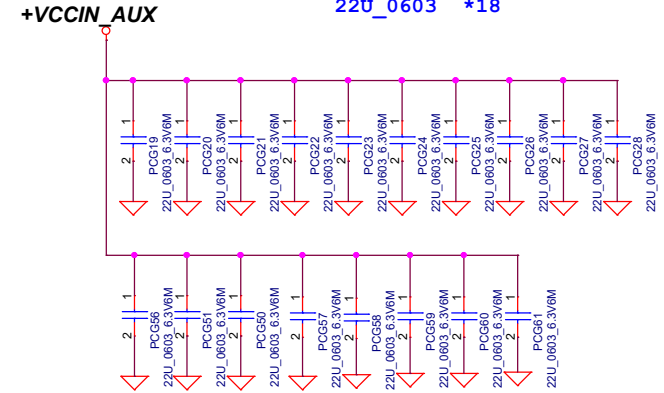
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Compal :
 Primary side :
 330U_R9 *1
 22U_0603 *20
 Back side:
 1U_0201 *6



330U_R9 *1
 22U_0603 *18

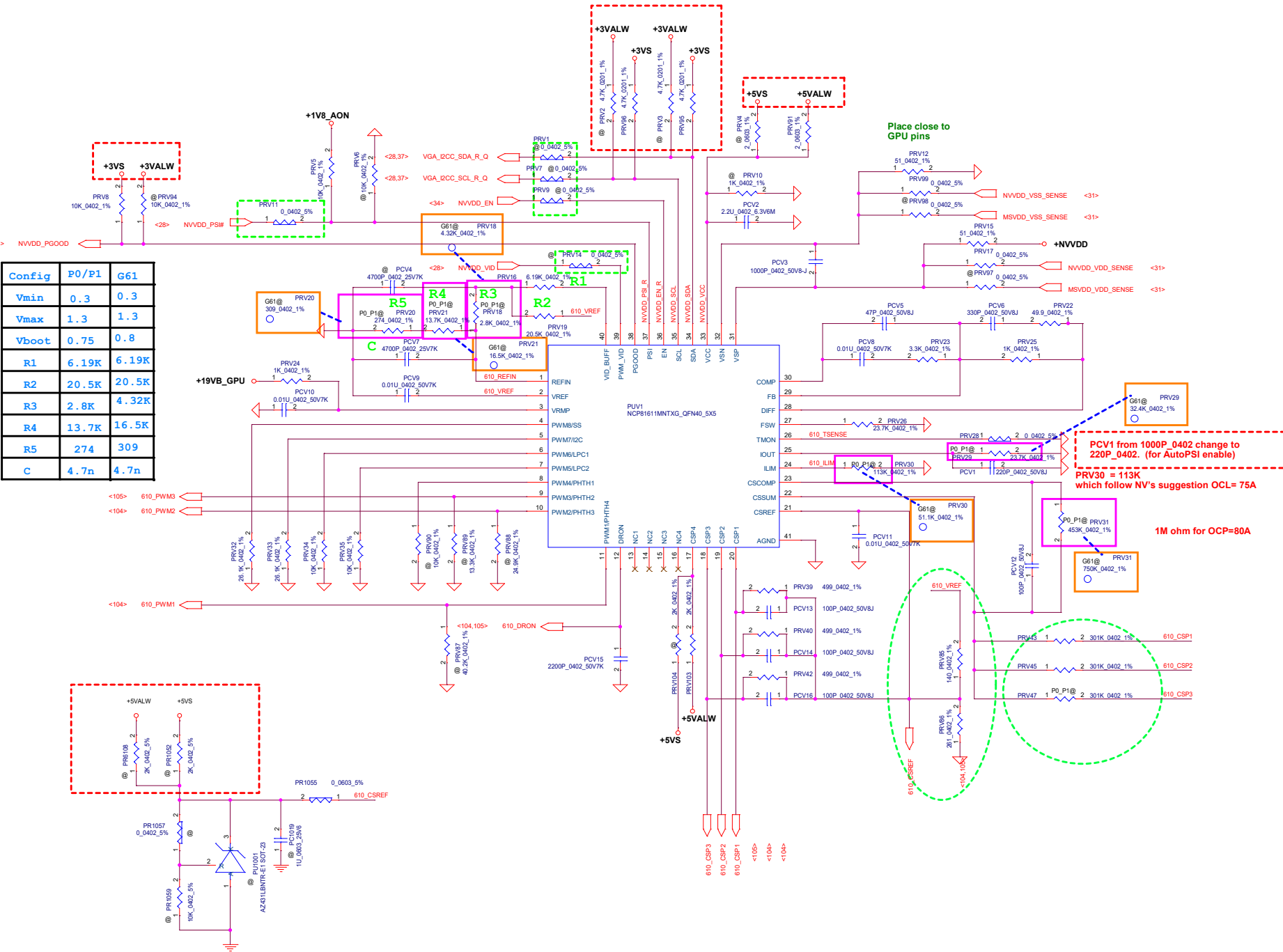


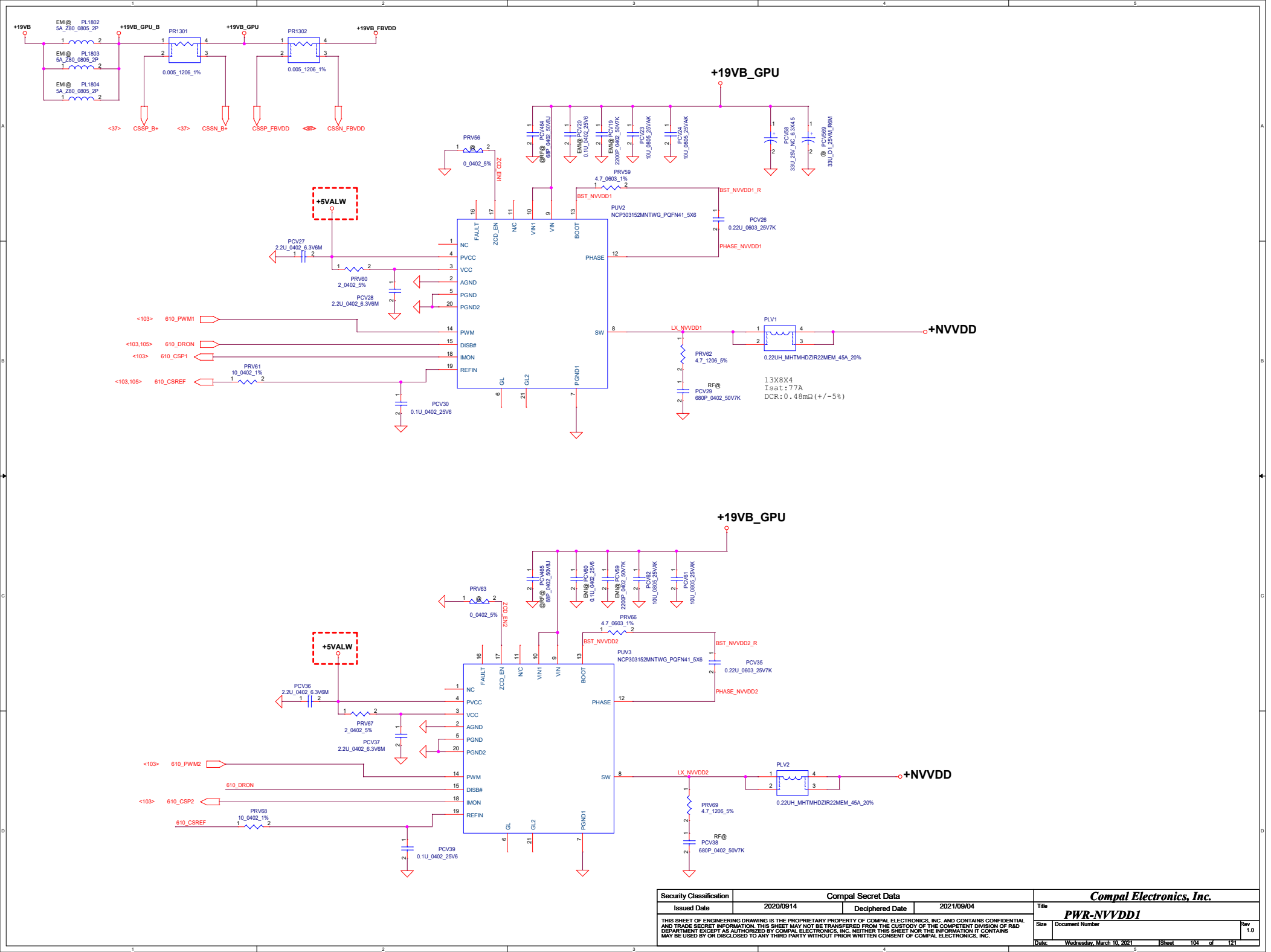
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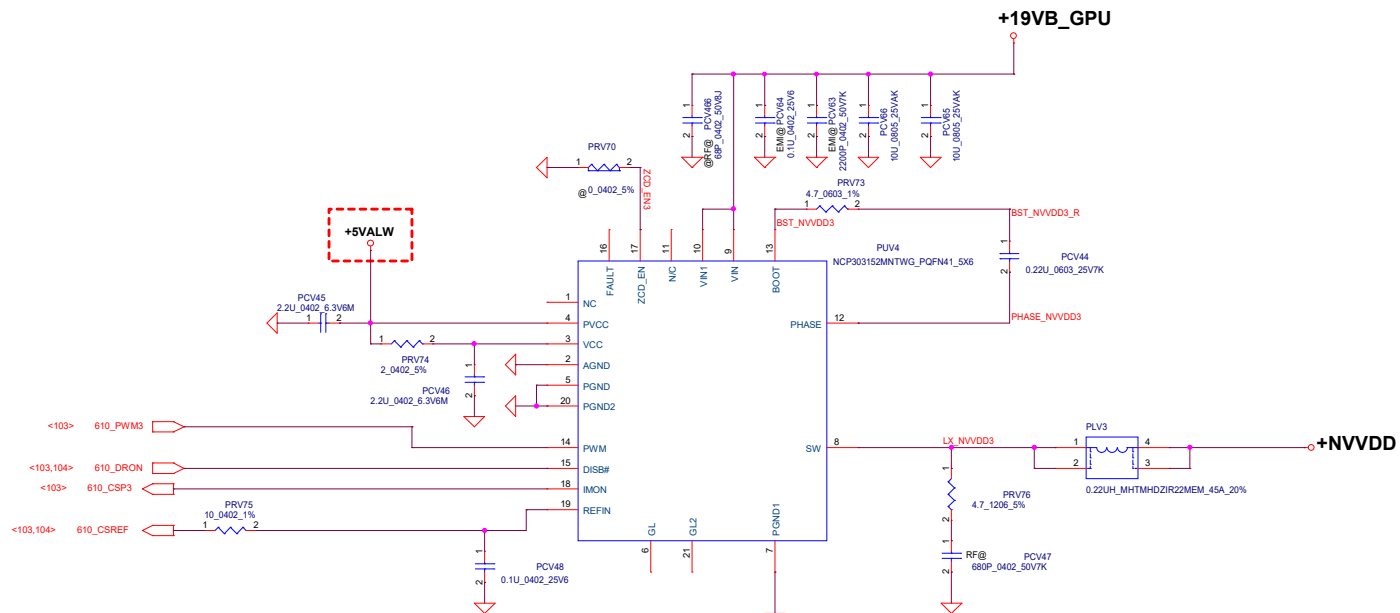
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Config	P0/P1	G61
Vmin	0.3	0.3
Vmax	1.3	1.3
Vboot	0.75	0.8
R1	6.19K	6.19K
R2	20.5K	20.5K
R3	2.8K	4.32K
R4	13.7K	16.5K
R5	274	309
C	4.7n	4.7n



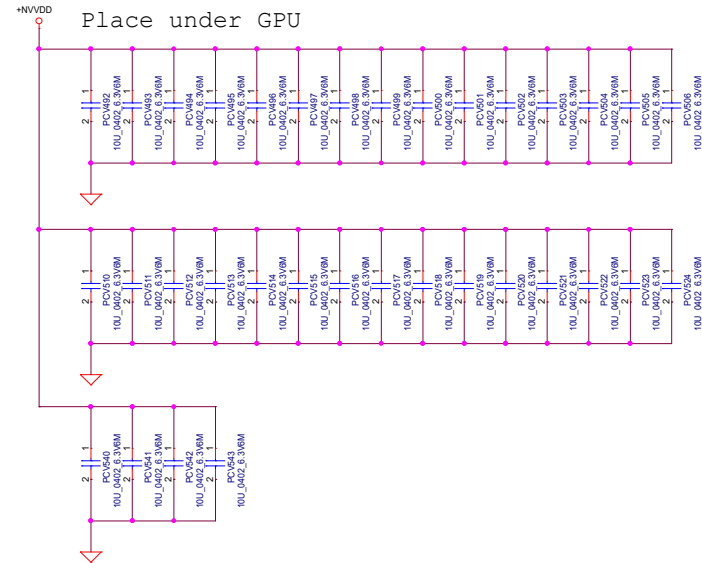
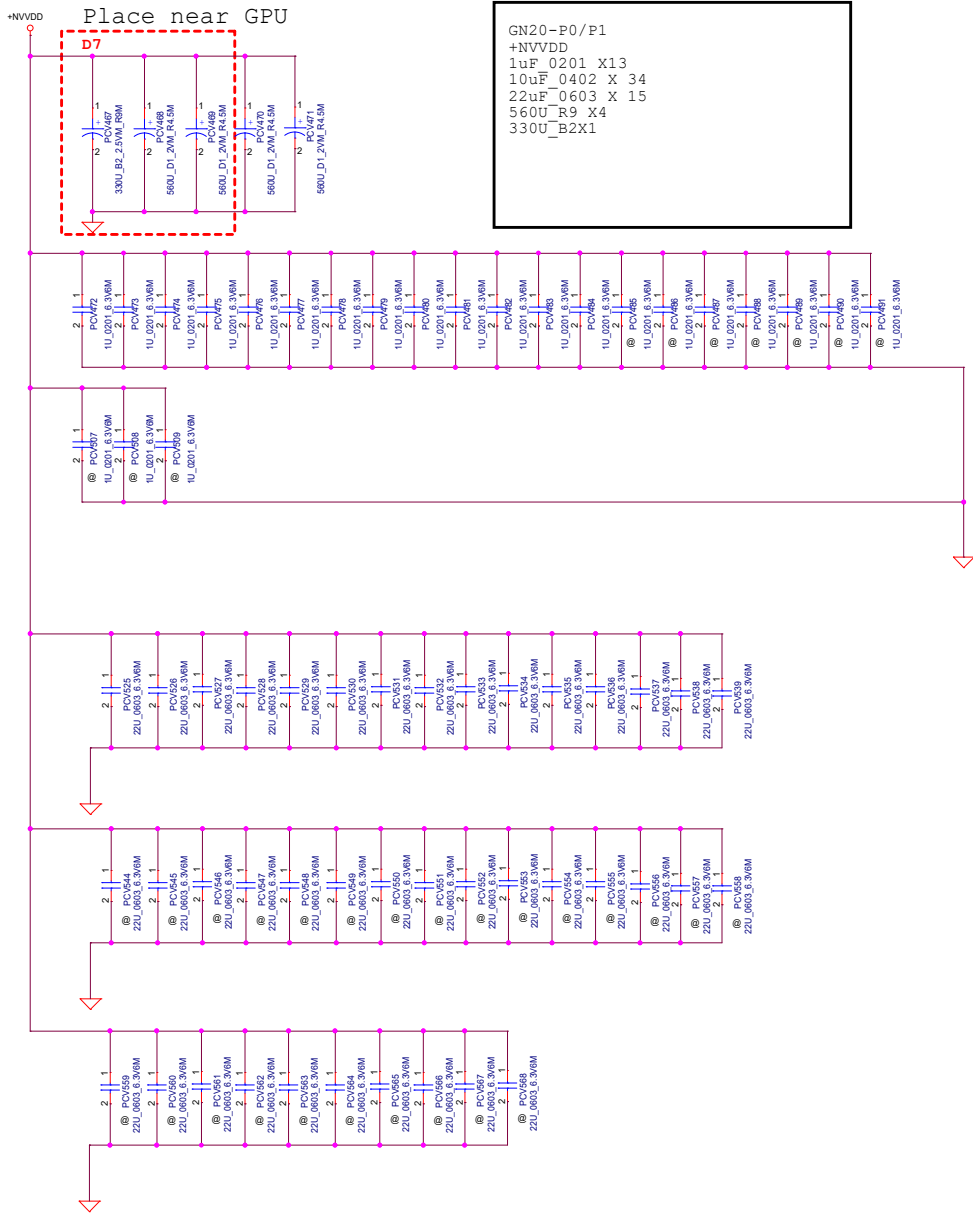




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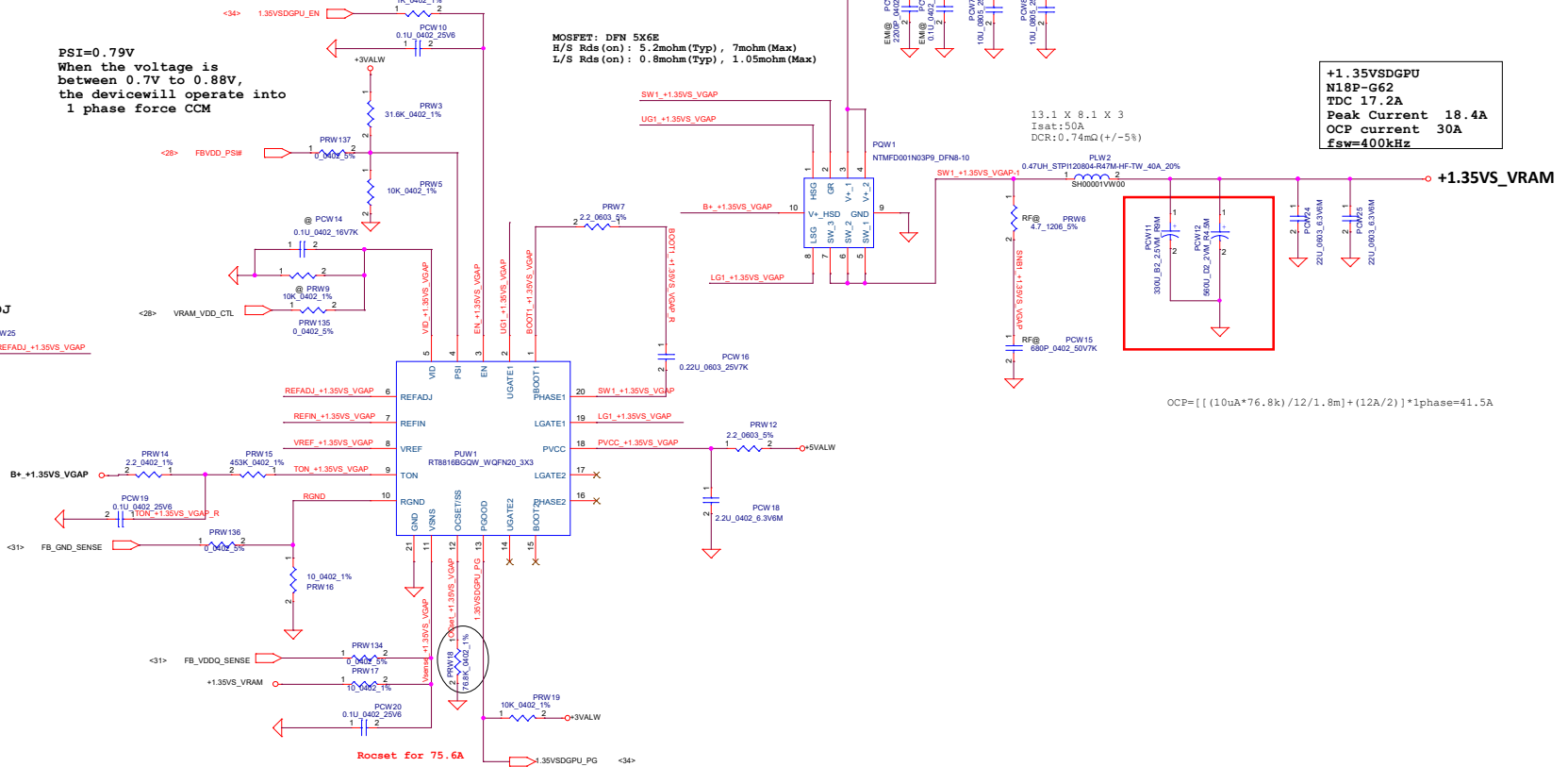
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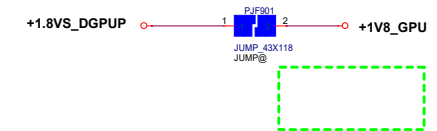
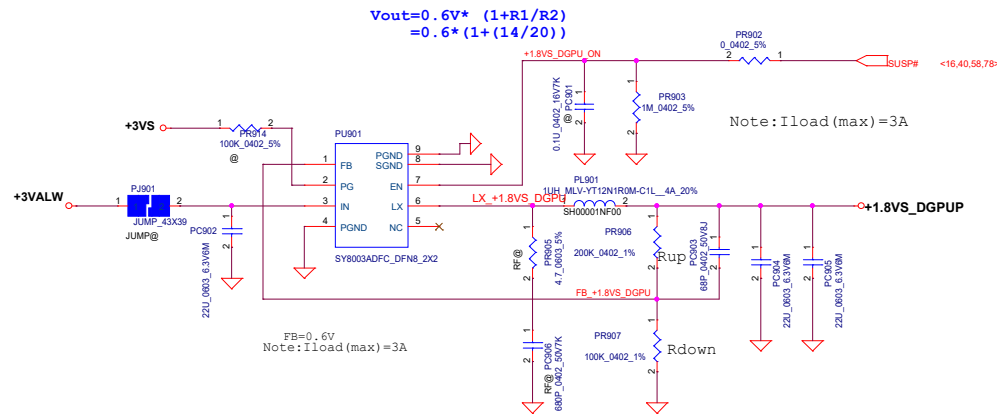
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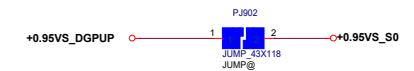
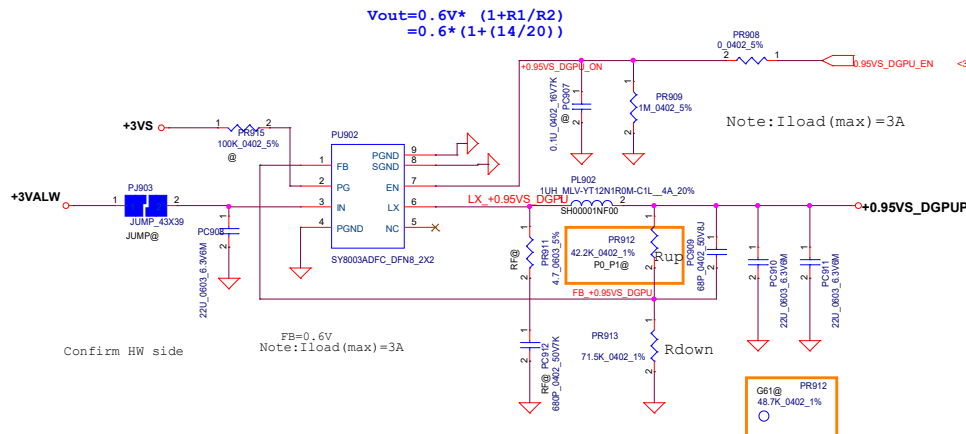
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Item	Reason for change	PG#	Modify List	Date	Phase
1	Change IC from 6A to 8A for design request	87	PU301 Change IC SY8386->SY8388	2020/11/3	SDV
2	Change choke for common design	85	PL2503 4.7uH -> 2.2uH	2020/11/3	SDV
3	Hw suggust to change for sequence	90	PC1801 mount PR1803 to 3.3k	2020/11/3	SDV
4	Change Capacitance for design request	107	PCV468 PCV469 PCV470 PCV471 330u to 560u	2020/11/3	SDV
5	Design circuit for battery FW	85	PQ311, PR335, PR336, PR338, PC9231	2020/11/3	SDV
6	Change resistor for common design	85	PR2507 0.01 -> 0.005 ohm	2020/11/12	SDV
7	Modify circuit for design request	103	add PRV103 2k Unmount PRV87 PRV88 PRV89 PRV1052 PRV1019 PRV1001 PRV26 41.2K ->23.7K PRV29 21.5K ->23.7K (P0P1) 32.4K (G61) PRV30 21.5K ->113K (P0P1) 51.1K (G61) PRV31 261K ->453K (P0P1) 750K (G61) PRV39 PRV40 PRV42 715 ->499 ohm PCV13 PCV14 PCV16 47p ->100p PRV85 PRV86 mount PRV6 unmount	2020/11/12	SDV
8	Change resistor for common design	88	PR514 52.3K ->> 84.5K	2020/11/12	SDV
9	Change resistor for common design	108	PRW23 7.87K ->>11K PRW25 35.7K ->> 100K	2020/11/12	SDV
10	Change Capacitance for common design	101	PCZ 16 unmount -> PCZ17 mount PCG50, PCG51, PCG56, PCG57, PCG58, PCG59, PCG60, PCG61 Mount	2020/11/12	SDV
11	Follow TI Spec design	85	PR350 PR351 1K-->0 ohm	2020/12/14	SIV
12	Change component for design	85	PC310 & PC9213 0.01u -> 0.1 u PQ311 Change P/N PC9207 Change 0603 -> 0402 (Sourcer recommend) PC9205 Change 0603 -> 0402 (Sourcer recommend)	2020/11/23	SIV
13	Change component for design	108	PQW1 AOS6932 ->AOS6930 PCW12 330u -> 560u PRW135 10K->0 ohm PRW24 25.5 K ->26.7K (Vram Voltage) PRW22 4.7K ->4.87K (Vram Voltage) PLW2 0.22uH ->0.47uH (for performance)	2020/12/14	SIV
14	Change component for design	103	PRV4 UNMOUNT -> PRV91 MOUNT (5VS -> 5VALW) PCV3 1000P Change P/N 25v->50v (Sourcer recommend)	2020/12/14	SIV
15	Follow NV Spec design	103	PRV97 PRV98 Unmount	2020/12/14	SIV
16	Change component for design	97	PRZ2 down size 0805 -> 0603 (Sourcer recommend) PRZ53 23.7K ->17.4K (for IMON) PRZ48 20K ->18.2K (for LL)	2020/12/14	SIV
17	Change component for design	87	PC302 1000P Change P/N (Sourcer recommend)	2020/12/14	SIV
18	Change component for design	110	PR912 42.2K ->48.7K (For G61 +1VS DGPUP)	2020/12/14	SIV
19	Change Compoent for design	104	PRV62 PRV69 PRV76 Change P/N (Sourcer recommend)	2020/12/14	SIV
20	Change Compoent for design	101	PCG 45 & PCG47 Change P/N (Sourcer recommend)	2020/12/14	SIV
21	Modify circuit for design request	82	add EMI@ PL206	2020/12/14	SIV

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